

## MAX77950

## WPC/PMA Dual Mode Wireless Power Receiver

### General Description

The MAX77950 is an advanced wireless power receiver IC that meets the specification requirements for WPC low-power (v1.2) and PMA SR1 (v2.0) communication protocols. This device operates using near-field magnetic induction when coupled with a WPC or PMA transmitter and provides output power up to 12 watts.

The IC has precision output current and voltage-sensing scheme over the entire load range. It enables accurate received power packets, as defined in the WPC specifications for best foreign object detection (FOD). The IC supports FSK demodulation to receive PMA advertisement ID as well as WPC FSK packets.

The IC features the patent-pending PeerPower™ function. In PeerPower mode, the IC operates as a transmitter, enabling power transfer to another peer device through in-band ASK communications.

The MAX77950 communicates with an application processor through an I<sup>2</sup>C serial interface. The status of power transfer and alerts are read through this interface.

### Applications

- Smartphones
- Tablets
- Smart Watches
- Headsets
- Wearable Devices
- Battery-Power Banks
- Wi-Fi Hotspots
- Digital Cameras
- Portable Medical Applications
- Portable Media Players
- Point-of-Sale Devices
- Handheld Devices

### Benefits and Features

- WPC/PMA Dual Mode Wireless Power Receiver
- Compliant with WPC Low Power (v1.2) and PMA SR1 (v2.0)
- Peer-to-Peer Power Transmission with In-Band ASK Communications
- WPC ASK Demodulator/FSK Demodulator
- Output Programmable Range from 3.5V to 12.7V with 100mV Step
- Integrated High-Efficiency n-Channel Full-Bridge Synchronous Rectifier
- Programmable Foreign Object Detection
- Programmable Dynamic Rectifier-Voltage Scaling
- Overvoltage, Overcurrent, and Overtemperature Protection

Ordering Information appears at end of data sheet.

*PeerPower is a trademark of Maxim Integrated Products, Inc.*

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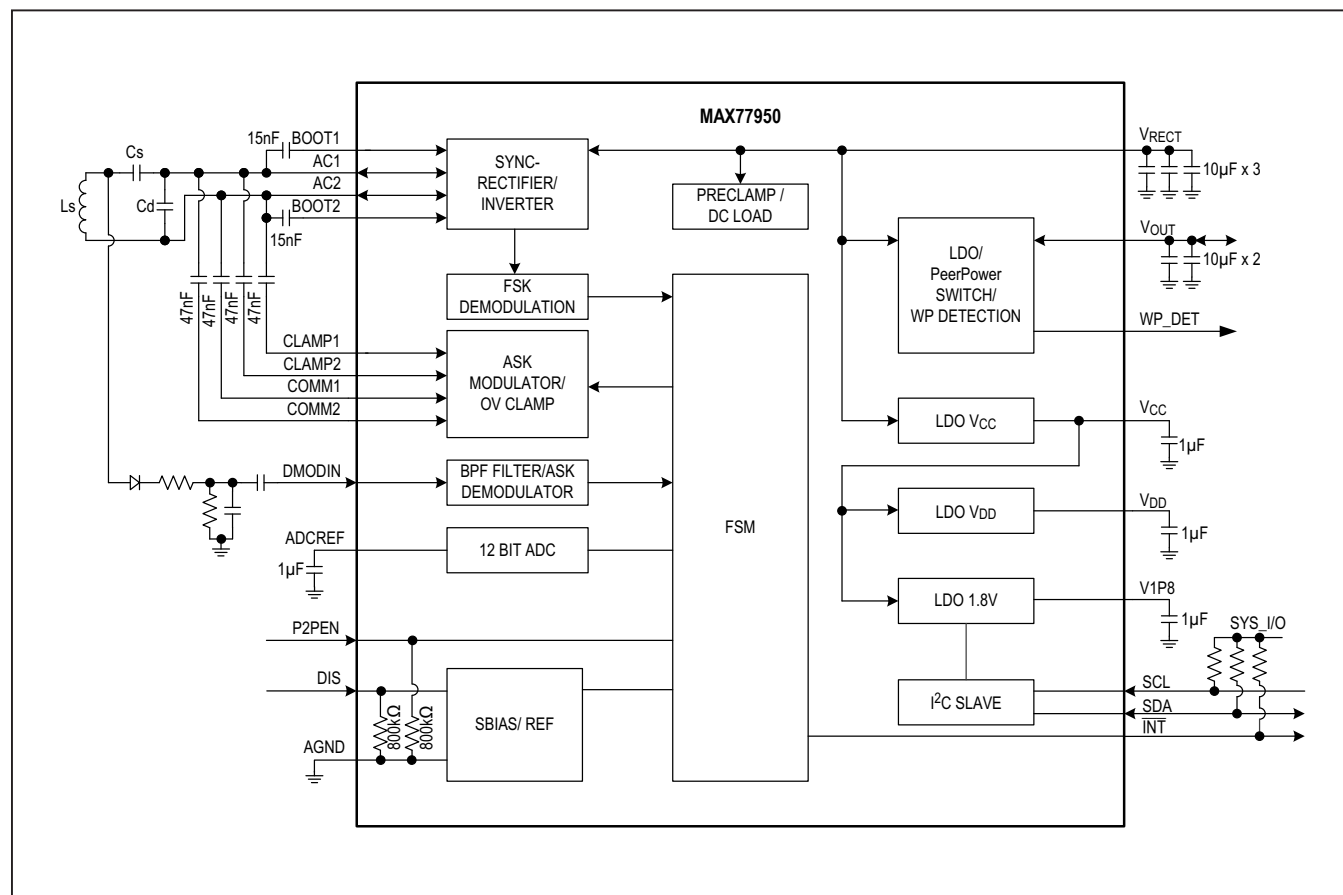
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## Simplified Block Diagram



## Absolute Maximum Ratings

AC1, AC2 to PGND .....-0.3V to +20V  
 VRECT, VOUT to PGND .....-0.3V to +20V  
 COMM1, COMM2, CLAMP1, CLAMP2 to PGND .....-0.3V to +20V  
 BST1, BST2 to PGND .....-0.3V to +25V  
 Differential ABS-MAX: BST1 to AC1, BST2 to AC2 .....+4.5V  
 VCC to AGND .....-0.3V to +4.5V  
 VDD to AGND .....-0.3V to +1.65V  
 V1P8 to AGND .....-0.3V to +4.5V  
 SCL, SDA, INT to AGND .....-0.3V to +4.5V  
 DIS to AGND .....-0.3V to V1P8 + 0.3V  
 WP\_DET to AGND .....-0.3V to V1P8 + 0.3V  
 P2PEN to AGND .....-0.3V to V1P8 + 0.3V

DMODIN to AGND .....-0.3V to VCC + 0.3V  
 ADCREF to AGND .....-0.3V to VDD + 0.3V  
 DNC .....-0.3V to VCC + 0.3V  
 AGND to PGND .....-0.3V to +0.3V  
 AC1, AC2 Current .....2.5A  
 VOUT Current .....-1.5A to +1.5A  
 COMM1, COMM2 .....1A  
 CLAMP1, CLAMP2 .....1.5A  
 Operating Ambient Temperature Range .....-40°C to +85°C  
 Junction Temperature .....-40°C to +150°C  
 Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

|                                              |                                                |
|----------------------------------------------|------------------------------------------------|
| Package Code                                 | W546A9+1 (6x9, 0.4mm pitch)                    |
| Outline Number                               | <a href="#">21-100082</a>                      |
| Land Pattern Number                          | <a href="#">Refer to Application Note 1891</a> |
| <b>THERMAL RESISTANCE, FOUR-LAYER BOARD:</b> |                                                |
| Junction to Ambient ( $\theta_{JA}$ )        | 40°C/W                                         |
| Junction to Case ( $\theta_{JC}$ )           | N/A                                            |

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{RECT}$  = 3V to 20V,  $T_A$  = -40°C to +85°C, unless otherwise noted, limits are 100% tested at  $T_A$  = +25°C; limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                             | SYMBOL                          | CONDITIONS                                                                              | MIN   | TYP   | MAX  | UNITS |
|-------------------------------------------------------|---------------------------------|-----------------------------------------------------------------------------------------|-------|-------|------|-------|
| Input Supply Current                                  | $I_{VRECT}$                     | No load                                                                                 |       | 5     |      | mA    |
| Disable Supply Current                                | $I_{VRECT\_SHDN}$               | DIS = 1, $V_{RECT}$ = 5V                                                                |       | 2.1   |      | mA    |
| Disable supply Current                                | $I_{VRECT\_SHDN}$               | DIS = 1, $V_{RECT}$ = 20V                                                               |       | 2.2   |      | mA    |
| Undervoltage Lockout Threshold                        | $V_{UVLO}$                      | $V_{RECT}$ rising                                                                       | 2.4   |       | 2.9  | V     |
| Undervoltage Lockout Hysteresis                       | $V_{UVLO\_HYS}$                 |                                                                                         |       | 400   |      | mV    |
| Internal Pulldown Resistance for DIS and P2PEN        | $R_{PD}$                        | Pulldown resistance to AGND                                                             | 400   | 800   | 1600 | kΩ    |
| <b>VOLTAGE REGULATORS</b>                             |                                 |                                                                                         |       |       |      |       |
| Voltage Regulator for Internal Blocks                 | $V_{CC}$                        |                                                                                         | 4.06  | 4.275 | 4.49 | V     |
|                                                       | $V_{DD}$                        |                                                                                         | 1.496 | 1.575 | 1.65 |       |
| V1P8 Voltage Regulator                                | V1P8                            | $I_{V1P8}$ = 20mA                                                                       | 1.71  | 1.8   | 1.89 | V     |
| <b>LDO</b>                                            |                                 |                                                                                         |       |       |      |       |
| HV LDO Input Voltage Range                            | $V_{RECT}$                      |                                                                                         | 3     |       | 20   | V     |
| $V_{OUT}$ Programmable Range Through I <sup>2</sup> C | $V_{OUTPRG}$                    | 100mV step                                                                              | 3.5   |       | 12.7 | V     |
| HV LDO Startup Rate                                   | $t_{LDOSTUP}$                   | $I_{OUT}$ = 0mA                                                                         |       | 0.5   |      | V/ms  |
| HV LDO Line Regulation                                | $\Delta V_{OUT}/\Delta V_{IN}$  | LDO_VOUTSET[6:0] = 0x32, $I_{OUT}$ = 1mA; $V_{RECT}$ = 6V to 12V                        |       | 0.1   |      | %     |
| HV LDO Load Regulation                                | $\Delta V_{OUT}/\Delta I_{OUT}$ | LDO_VOUTSET[6:0] = 0x32, $I_{OUT}$ = 1mA to 1A, $V_{RECT}$ = 5.2V                       |       | 0.5   |      | %     |
| HV LDO Load Transient                                 |                                 | $I_{OUT}$ = 1mA to 1A and 1A to 1mA within 20μs                                         |       | ±8    |      | %     |
| HV LDO Dropout Voltage                                | $V_{DO}$                        | LDO_VOUTSET[6:0] = 0x32, $I_{OUT}$ = 1A, $V_{DO}$ = $V_{RECT} - V_{OUT}$                |       |       | 100  | mV    |
| HV LDO Current Limit                                  | $I_{LIM}$                       | LDO_ILIMSET[4:0] = 0x1A, LDO_VOUTSET[6:0] = 0x32, $V_{RECT}$ = +5.1V, $V_{OUT}$ = +4.8V | 1.1   |       | 1.5  | A     |
| Output Voltage Initial Accuracy                       | $V_{OUT\_ACC}$                  | LDO_VOUTSET[6:0] = 0x32, $I_{OUT}$ = 1mA, $T_A$ = +25°C                                 | -2    |       | +2   | %     |
| <b>COMM PINS</b>                                      |                                 |                                                                                         |       |       |      |       |
| COMMn On-Resistance                                   | $R_{COMM}$                      |                                                                                         |       | 1     |      | Ω     |
| COMMn Leakage Current                                 | $I_{COMM}$                      | $V_{COMM1}$ = $V_{COMM2}$ = 20V, $T_A$ = +25°C                                          |       |       | 1    | μA    |
| <b>CLAMP PINS</b>                                     |                                 |                                                                                         |       |       |      |       |
| CLAMPn On-Resistance                                  | $R_{CLAMP}$                     |                                                                                         |       | 0.5   |      | Ω     |
| CLAMPn Leakage Current                                | $I_{CLAMP}$                     | $V_{CLAMP1}$ = $V_{CLAMP2}$ = 20V, $T_A$ = +25°C                                        |       |       | 1    | μA    |
| OVP Preclamp Threshold                                | OVLOPRECLAMP                    | $V_{RECT}$ rising                                                                       |       | 16    |      | V     |



## Electrical Characteristics (continued)

( $V_{RECT}$  = 3V to 20V,  $T_A$  = -40°C to +85°C, unless otherwise noted, limits are 100% tested at  $T_A$  = +25°C; limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                    | SYMBOL            | CONDITIONS                                                         | MIN        | TYP  | MAX   | UNITS |
|----------------------------------------------|-------------------|--------------------------------------------------------------------|------------|------|-------|-------|
| <b>SYNCHRONOUS RECTIFIER</b>                 |                   |                                                                    |            |      |       |       |
| High-Side Switch On-Resistance               | $R_{ON\_HS}$      |                                                                    |            | 50   |       | mΩ    |
| Low-Side Switch On-Resistance                | $R_{ON\_LS}$      |                                                                    |            | 50   |       | mΩ    |
| <b>ADC</b>                                   |                   |                                                                    |            |      |       |       |
| ADC Reference Voltage                        | $V_{ADC\_REF}$    | No load                                                            | 1.237      | 1.25 | 1.262 | V     |
| Initial ADC Accumulated Error for $V_{RECT}$ | $ADC\_ERR\_VRECT$ | $V_{RECT}$ = 3V to 15V, production tested at 3.5V, 7.5V, and 14.5V | -1         |      | +1    | %     |
| Initial ADC Accumulated Error for $V_{OUT}$  | $ADC\_ERR\_VOUT$  | $V_{OUT}$ = 3.6V to 10V, production tested at 3.5V, 6.5V, and 9.5V | -1         |      | +1    | %     |
| Initial ADC Accumulated Error for $I_{SNS}$  | $ADC\_ERR\_ISNS$  | Current range 0 to 1A, $T_A$ = +25°C                               | -10        |      | +10   | mA    |
| <b>DEMODULATOR</b>                           |                   |                                                                    |            |      |       |       |
| DMODIN Input Resistance                      |                   |                                                                    |            | 0.7  |       | mΩ    |
| DMODIN Minimum Detectable Input Voltage      |                   |                                                                    | 200        |      |       | mV    |
| <b>THERMAL PROTECTION</b>                    |                   |                                                                    |            |      |       |       |
| Thermal Shutdown                             | $T_{JOFF}$        | $T_J$ rising                                                       |            | 165  |       | °C    |
| Thermal-Shutdown Hysteresis                  | $T_{JOFFHYS}$     | $T_J$ falling                                                      |            | 10   |       | °C    |
| Temperature-Warning Threshold                | $T_{JWARN}$       |                                                                    |            | 120  |       | °C    |
| <b>LOGIC OUTPUT</b>                          |                   |                                                                    |            |      |       |       |
| WP_DET Output High Voltage                   |                   | Source current 5mA                                                 | V1P8 - 0.4 |      |       | V     |
| WP_DET Output Low Voltage                    |                   | Sink current 5mA                                                   |            |      | 0.4   | V     |
| INTB Output Low Voltage                      | $V_{OL}$          | Sink current 20mA                                                  |            |      | 0.4   | V     |
| <b>LOGIC INPUT</b>                           |                   |                                                                    |            |      |       |       |
| P2PEN Input High Voltage                     |                   |                                                                    | 1.4        |      |       | V     |
| P2PEN Input Low Voltage                      |                   |                                                                    |            |      | 0.4   | V     |
| P2PEN Input Leakage Current                  |                   |                                                                    |            |      | 1     | μA    |
| DIS Input High Voltage                       |                   |                                                                    | 1.4        |      |       | V     |
| DIS Input Low Voltage                        |                   |                                                                    |            |      | 0.4   | V     |
| DIS Input Leakage Current                    |                   |                                                                    |            |      | 1     | μA    |

## Electrical Characteristics (continued)

( $V_{RECT} = 3V$  to  $20V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted, limits are 100% tested at  $T_A = +25^{\circ}C$ ; limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                      | SYMBOL        | CONDITIONS                                                                | MIN | TYP | MAX | UNITS   |
|------------------------------------------------|---------------|---------------------------------------------------------------------------|-----|-----|-----|---------|
| <b>I<sup>2</sup>C INTERFACE</b>                |               |                                                                           |     |     |     |         |
| SCL, SDA Input High Voltage                    | $V_{IH}$      |                                                                           | 1.4 |     |     | V       |
| SCL, SDA Input Low Voltage                     | $V_{IL}$      |                                                                           |     |     | 0.4 | V       |
| SCL, SDA Input Hysteresis                      | $V_{HYS}$     |                                                                           |     | 0.2 |     | V       |
| SCL, SDA Input Leakage Current                 | $I_I$         | $0.1 \times V_{DD} < SCL/SDA < 0.9 \times V_{DD}$                         | -1  |     | +1  | $\mu A$ |
| SDA Output Low Voltage                         | $V_{OL}$      | Sinking 10mA                                                              |     |     | 0.4 | V       |
| SCL, SDA Pin Capacitance                       | $C_I$         |                                                                           |     | 10  |     | pF      |
| Output Fall Time from $V_{IH}$ to $V_{IL}$     | $t_{OF}$      |                                                                           |     |     | 300 | ns      |
| Clock Frequency                                | $f_{SCL}$     |                                                                           | 0   |     | 400 | kHz     |
| Hold Time Repeated Start Condition             | $t_{HD:STA}$  | Note 4                                                                    | 0.6 |     |     | $\mu s$ |
| SCL Low Period                                 | $t_{LOW}$     |                                                                           | 1.3 |     |     | $\mu s$ |
| SCL High Period                                | $t_{HIGH}$    |                                                                           | 0.6 |     |     | $\mu s$ |
| Setup Time Repeated Start Condition            | $t_{SU\_STA}$ |                                                                           | 0.6 |     |     | $\mu s$ |
| Data Hold Time                                 | $t_{HD\_DAT}$ | Note 5                                                                    | 0   |     | 0.9 | $\mu s$ |
| Data Setup Time                                | $t_{SU\_DAT}$ |                                                                           | 100 |     |     | ns      |
| Setup Time for STOP Condition                  | $t_{SU\_STO}$ |                                                                           | 0.6 |     |     | $\mu s$ |
| Bus Free Time Between STOP and START Condition | $t_{BUF}$     |                                                                           | 1.3 |     |     | $\mu s$ |
| Data Valid Time                                | $t_{VD:DAT}$  |                                                                           |     |     | 0.9 | $\mu s$ |
| Data Valid Acknowledge Time                    | $t_{VD:ACK}$  |                                                                           |     |     | 0.9 | $\mu s$ |
| Bus Capacitance                                | $C_B$         |                                                                           |     |     | 550 | pF      |
| Pulse Width of Suppressed Spikes               | $t_{SP}$      | Maximum pulse width of spikes that must be suppressed by the input filter |     | 50  |     | ns      |

**Note 1:** Limits are 100% production tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 2:** All voltages are referenced to AGND.

**Note 3:** Test is performed on unmounted/unsoldered ports.

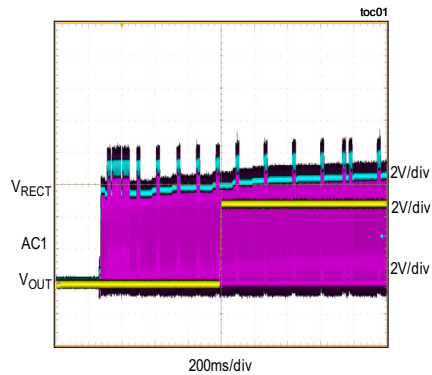
**Note 4:**  $f_{SCL}$  must meet the minimum clock low time plus the rise/fall times.

**Note 5:** The maximum  $t_{HD:DAT}$  has to be met only if the device does not stretch the low period ( $t_{LOW}$ ) of the SCL signal.

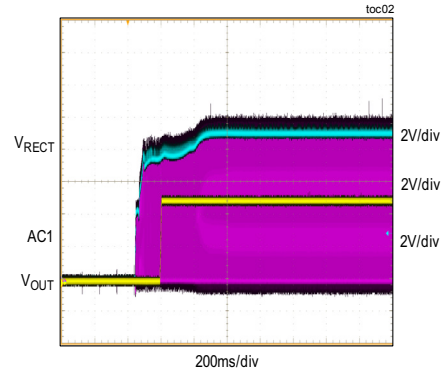
## Typical Operating Characteristics

(Using WPC A11 and PMA 7 transmitters at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

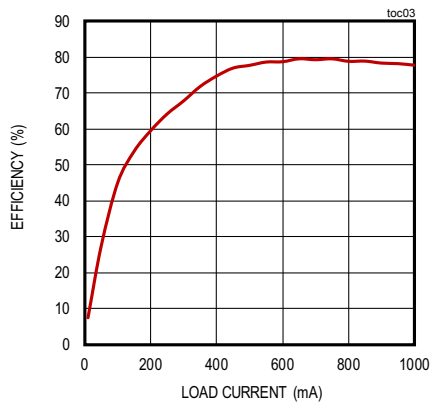
WPC MODE NO LOAD START-UP



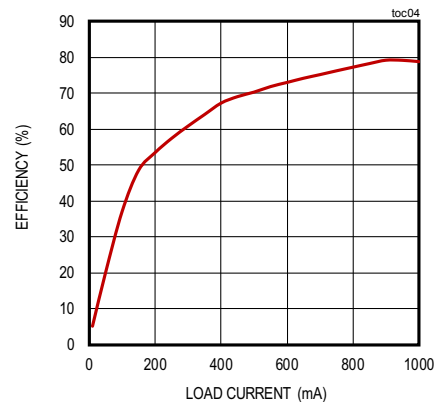
PMA MODE NO LOAD START-UP



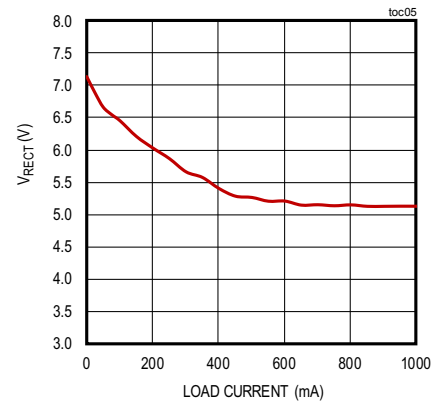
WPC MODE DC-DC EFFICIENCY



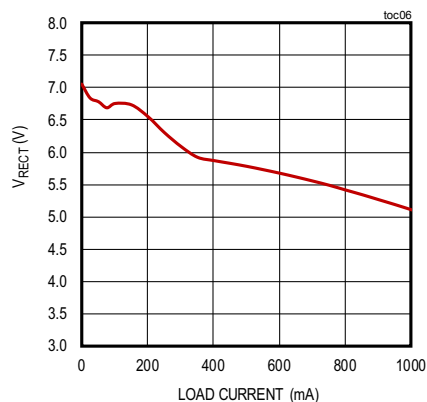
PMA MODE DC-DC EFFICIENCY



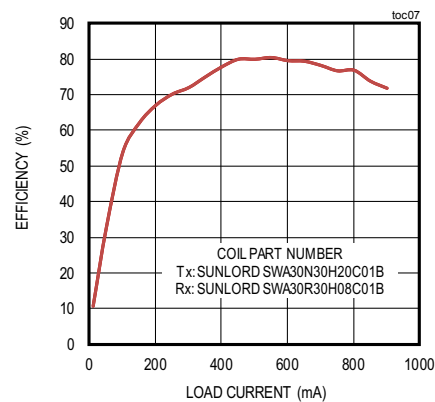
RECTIFIER VOLTAGE IN WPC MODE



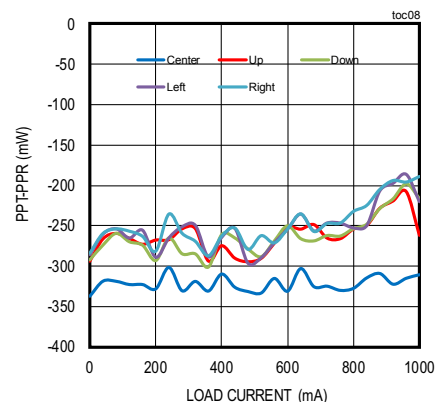
RECTIFIER VOLTAGE IN PMA MODE



PeerPower MODE DC-DC EFFICIENCY

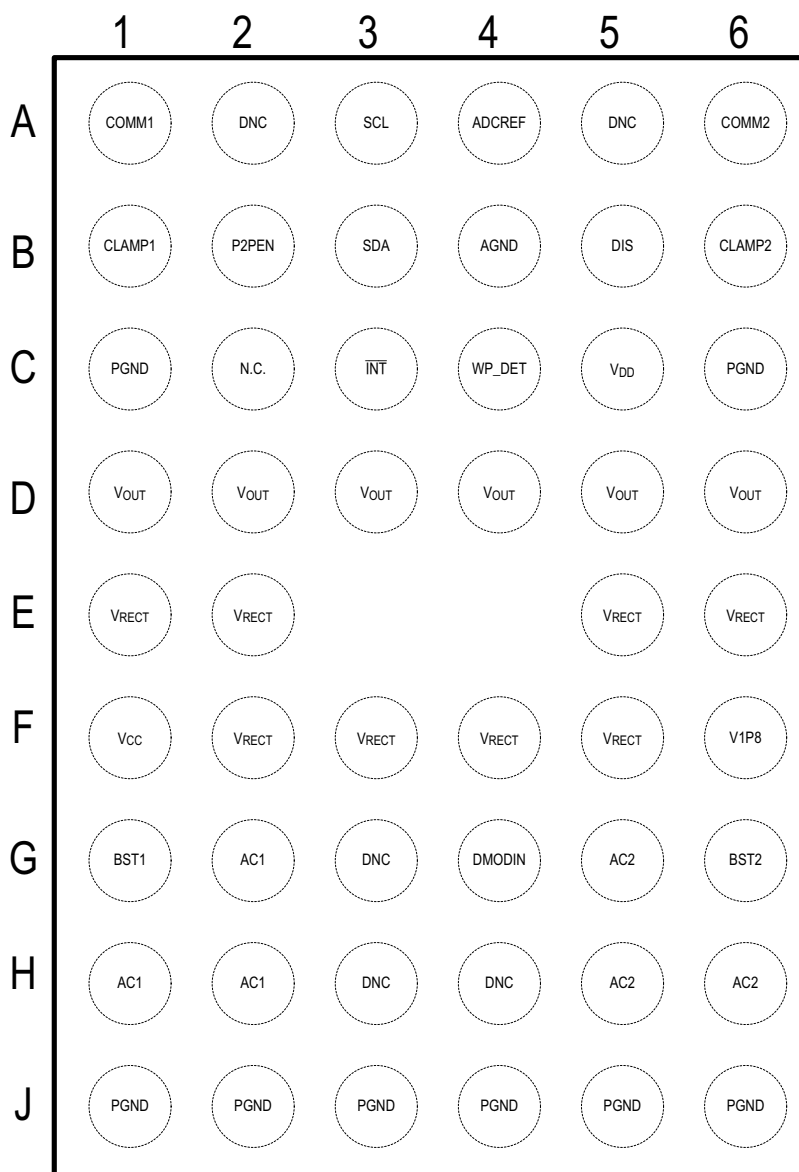


WPC FOREIGN OBJECT DETECTION



## Bump Configuration

TOP VIEW  
(BUMP SIDE DOWN)



( 52-Bump WLP, 0.4mm pitch )

## Bump Description

| PIN                   | NAME              | FUNCTION                                                                                                                       | TYPE           |
|-----------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------|----------------|
| A1                    | COMM1             | Open-Drain Output. Achieves the AC modulation to communicate with the Tx.                                                      | Digital Output |
| A2, A5, G3, H3, H4    | DNC               | Do Not Connect. Leave open in system.                                                                                          | Analog I/O     |
| A3                    | SCL               | I <sup>2</sup> C Clock Input                                                                                                   | Digital Input  |
| A4                    | ADCREF            | ADC Reference Voltage. Bypass to ground with a 1μF ceramic capacitor.                                                          | Analog Output  |
| A6                    | COMM2             | Open-Drain Output. Achieves the AC modulation to communicate with the Tx.                                                      | Digital Output |
| B1                    | CLAMP1            | Open-Drain Outputs. Switches to modulate ASK to communicate with Tx. Turns on when V <sub>RECT</sub> overvoltage event occurs. | Digital Output |
| B2                    | P2PEN             | PeerPower function active-high enable input.                                                                                   | Digital Input  |
| B3                    | SDA               | I <sup>2</sup> C Data Input/Output                                                                                             | Digital I/O    |
| B4                    | AGND              | Analog Reference Ground. "Star-ground" connection to system GND.                                                               | Ground         |
| B5                    | DIS               | Disable Pin, Active-High                                                                                                       | Digital Input  |
| B6                    | CLAMP2            | Open-Drain Outputs. Switches to modulate ASK to communicate with Tx. Turns on when V <sub>RECT</sub> overvoltage event occurs. | Digital Output |
| C1, C6, J1– J6        | PGND              | Power Ground                                                                                                                   | Ground         |
| C2                    | N.C.              | Not Internally Connected. Can connect to power, ground, or leave open.                                                         | No Connect     |
| C3                    | INT               | Open-Drain, Active-Low Interrupt Output                                                                                        | Digital Output |
| C4                    | WP_DET            | Wireless Power Detected Output. Active-high                                                                                    | Digital Output |
| C5                    | V <sub>DD</sub>   | +1.575V linear regulator low ripple output for internal use. Bypass to ground with a 1μF ceramic capacitor.                    | Power Output   |
| D1–D6                 | V <sub>OUT</sub>  | Linear Regulator Output. Bypass to ground with two 10μF capacitors.                                                            | Power I/O      |
| E1, E2, F2–F5, E5, E6 | V <sub>RECT</sub> | Rectifier's Output. Bypass to ground with three 10μF and one 100nF ceramic capacitor.                                          | Power I/O      |
| F1                    | V <sub>CC</sub>   | +4.275V linear regulator low ripple output for internal use. Bypass to ground with a 1μF ceramic capacitor.                    | Power Output   |
| F6                    | V1P8              | +1.8V linear regulator low ripple output. Bypass to ground with a 1μF ceramic capacitor.                                       | Power Output   |
| G1                    | BST1              | Bootstrap pin for rectifier's high side n-channel FET gate driver.                                                             | Analog Output  |
| G2, H1, H2            | AC1               | Rectifier Input. Connect to receiver LC tank.                                                                                  | Power Input    |
| G4                    | DMODIN            | Amplitude Shift Keying Demodulator Input                                                                                       | Analog Input   |
| G5, H5, H6            | AC2               | Rectifier Input. Connect to receiver LC tank.                                                                                  | Power Input    |
| G6                    | BST2              | Bootstrap pin for rectifier's high side n-channel FET gate driver                                                              | Analog Output  |

The MAX77950 block diagram illustrates the internal architecture of the chip, which is designed for WPC/PMA Rx functionality. The central component is the **MAIN FSM FOR WPC/PMA Rx FUNCTIONALITY**, which coordinates the operation of various internal blocks.

**Power Management and Input/Output:**

- Power Input:** The chip has multiple **VRECT** pins for rectified input. It also features **PGND** pins for ground connection.
- Power Regulation:** The **HV-LDO / PeerPower SWITCH** block regulates the input voltage. It includes an **ISNS** (sense) pin and an **ILIM** (limit) pin. The output is connected to **VOUT** pins.
- Reference and Bias:** A **VREF** pin provides a reference voltage. The **BIAS, BG/ SBIAS** block provides biasing for the internal circuitry, with a **TDIE** (temperature-dependent internal error) pin.
- Output:** The chip has multiple **VOUT** pins for the regulated output.

**Signal Processing and Control:**

- Rectification and Inversion:** The **RECTIFIER/ INVERTER CONTROLLER** and **SYNC-RECTIFIER / INVERTER** blocks handle the initial signal processing, involving transistors **Q1, Q2, Q3, Q4**.
- Demodulation and Modulation:** The **FSK DEMOD FSM** and **ASK MODULATOR** blocks handle the FSK and ASK signals. The **AFE ASK DEMODULATOR** block is also present.
- Filtering:** **LOWPASS FILTER** and **HIGHPASS FILTER** blocks are used for signal conditioning.
- Control and Test:** The **TEST CONTROLLER** block manages the chip's test functions. The **ADC SEQUENCER** and **12-BIT ADC** block handle analog-to-digital conversion. The **REGISTER BANK** and **OTP** (One-Time Programmable) block store configuration data.
- Communication:** The **I2C SLAVE** block allows for external communication via **SCL** and **SDA** pins.

**External Components and Connections:**

- Capacitors:** Various capacitors are shown, including **C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695**

## Detailed Description

### Wireless Power Transfer System Overview

A wireless power system consists of a base station on the primary side and a power receiver on the secondary side, as shown in [Figure 1](#). The base station (referred to as a power transmitter), comprises a power conversion unit, primary coil, communications demodulator, and control unit. The power receiver comprises a secondary coil, power pick-up unit, communications modulator, and controller.

When the receiver is placed on top of the transmitter's interface surface, the magnetic field that is generated by the primary coil induces a voltage on the secondary coil when the coils are magnetically coupled together. The output voltage of the receiver is regulated, and the received power is controlled through the communications and control unit in the receiver. The receiver communicates with the transmitter for requesting increased power, decreased power, no change in power transfer, or power-transfer termination. This communication is conducted in-band between the coils and is digitally overlaid on top of the power signal. The impedance on the secondary side

is modulated as the receiver communicates, which is captured as load modulation by the primary coil. The transmitter changes frequency, duty cycle, or even voltage input of the power inverter to meet the demand of power that the receiver requests through the communication.

In WPC mode, the transmitter detects the modulation of the current and/or voltage across the primary coil and demodulates communication messages known as packets. A few examples of WPC packets are control error packet, received power packet, and end power transfer packet. The digital communication scheme, in the WPC protocol, utilizes differential bi-phase encoding as ONE and ZERO bits are transferred from the secondary to primary at a rate of 2kbps.

The PMA communication protocol operates continuously to transmit symbol messages that are encoded through frequency-based modulation. The receiver can send six different types of symbols to the transmitter using different frequency rates between 250Hz and 8kHz. They include decrement (DEC), increment (INC), no change (NoCh), end of charge (EOC), MsgBit, and a proprietary symbol intended for future use.

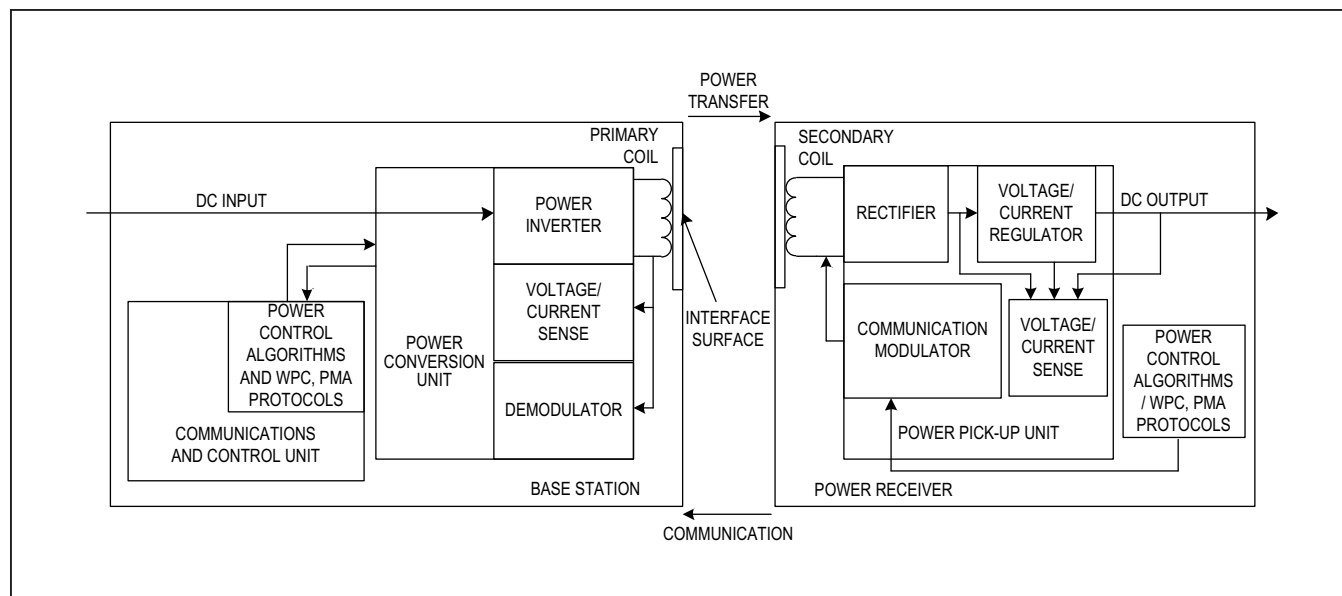


Figure 1. Wireless Power Transfer System Diagram

### Rectified-Voltage Control Loop

The rectified voltage ( $V_{RECT}$ ) is regulated by a closed control loop between the wireless power transmitter (base station) and the wireless power receiver (mobile device). To achieve the best compromise between optimal efficiency and output load transient response, the rectified voltage is regulated based on the output current. The  $V_{RECT}$  profile versus the load can be programmed in the following user registers, as shown in [Figure 2](#).

The  $V_{RECT}$  target voltage is stored in eight 8-bit registers allocated for WPC mode ( $V_{RECT\_TARGET\_Y0}$  to  $V_{RECT\_TARGET\_Y7}$ ) and eight 8-bit registers allocated for PMA mode ( $V_{RECT\_TARGET\_PMA\_Y0}$  to  $V_{RECT\_TARGET\_PMA\_Y7}$ ). The output current is divided into eight thresholds which are stored in the registers  $V_{RECT\_TARGET\_X0}$  to  $V_{RECT\_TARGET\_X7}$ . Different  $V_{RECT}$  target profiles are used for WPC and PMA due to the different power transfer profile characteristics.

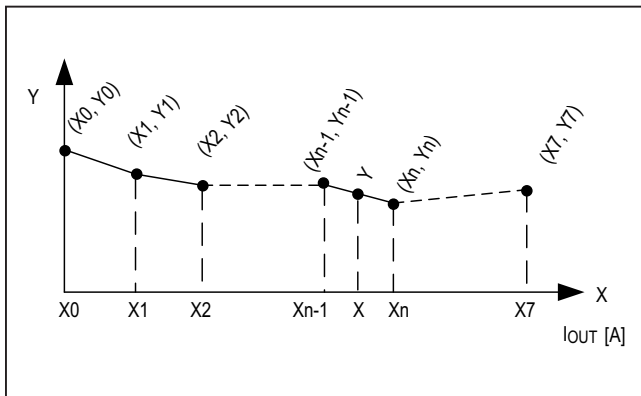


Figure 2. Rectified Voltage Profile vs. Output Current

The following equation calculates the  $V_{RECT}$  target based on linear interpolation between the adjacent coefficients:

$$y = y_{n-1} + \frac{(x - x_{n-1})(y_n - y_{n-1})}{x_n - x_{n-1}}$$

Where X is the actual output current reading:

$$V_{RECT\_TARGET\_X_n} = \frac{X_n(A) \times 255 \times 0.73}{1.25}$$

$$V_{RECT\_TARGET\_Y_n} = \frac{Y_n(V) \times 255}{1.25 \times 12}$$

$$V_{RECT\_TARGET\_PMA\_Y_n} = \frac{Y_n(V) \times 255}{1.25 \times 12}$$

### PeerPower Function

#### Overview

The PeerPower function enables one mobile device to charge another mobile device wirelessly. [Figure 3](#) shows the main concept.

The MAX77950 is a highly configurable wireless power IC that allows the user to reconfigure the rectifier into a full-bridge inverter, achieving high-efficiency power transfer due to low  $R_{DS(ON)}$  of the power MOSFETs.

Once P2PEN is pulled high, the switch located between  $V_{OUT}$  and  $V_{RECT}$  is turned on and the inverter generates a digital ping repeatedly. The IC continues power transfer once it receives the signal strength packet and also terminates power transfer after the end power transfer packet is received. A demodulated packet is stored in the registers (such as  $TX\_WPC\_HEADER$ ,  $TX\_WPC\_DATA0/..7$ ) until the next packet comes.

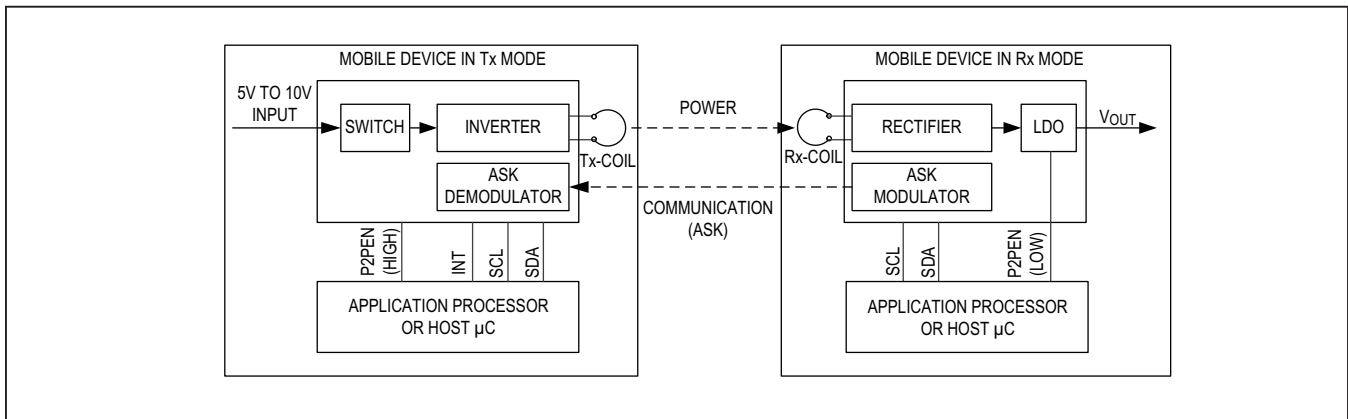


Figure 3. System-Level Block Diagram in PeerPower Mode



In PeerPower mode, the IC can generate interrupts in power transfer phase whenever it receives WPC packets that are non-zero CEP, RPP, CSP, EPT, and PPP so that an application processor or microcontroller notices it. To make this, a user needs to enable the ASK\_DEMOD\_PT\_INT\_EN bit. Then, INT goes low and the ASK\_DEMOD\_PT bit is set whenever the IC receives packets in power transfer phase.

To operate the IC in PeerPower mode, the following steps must be followed:

- 1) Supply an input voltage to the output of the LDO ( $V_{OUT}$  pin).
- 2) Program initial frequency into TX\_FOP\_SET\_H/L; otherwise, the inverter will operate at 125kHz since it is the default frequency.
- 3) Pull P2PEN pin high to make LDO be a switch and run the inverter.

### Wireless Power Detection Function

The IC offers a WP\_DET output that is a power-good indicator that monitors the  $V_{OUT}$  level. The WP\_DET output goes high once  $V_{OUT}$  exceeds the level programmed in WPDET\_H\_Threshold[1:0] and it goes low once  $V_{OUT}$  drops down to the level programmed in WPDET\_L\_Threshold[1:0].

### Clamp Function

An overvoltage event may occur when the mobile device is moved over the transmitter's surface, or when partially removed from the mobile device and quickly placed on the power transmitter. In addition, it may occur during the ping stage in PMA mode. The IC has preclamp and clamp features to limit the rectifier-output voltage as an overvoltage protection. The preclamp pulls 250mA from  $V_{RECT}$  to PGND when the voltage on  $V_{RECT}$  exceeds 16V. If the rectifier-output voltage reaches 17V, even after the preclamp is activated, the IC turns on FETs between CLAMP1/2 and PGND as an additional protection. The preclamp and the clamp thresholds are both programmable through I2C.

### ASK/FSK Demodulation

The IC contains an ASK demodulation block that demodulates WPC ASK in PeerPower mode. In WPC, transmitted power is coupled to the receiver coil. When the receiver is powered up, it communicates with the transmitter at 2kHz

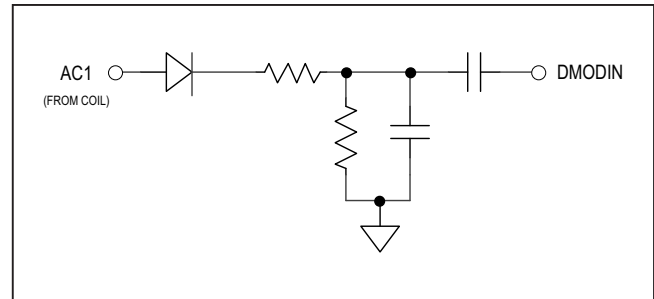


Figure 4. External Circuits for Envelope Detection, Level Shifting, and AC Coupling

by modulating the impedance of the receiver coil with communication capacitors. The function of the IC's ASK demodulator is to detect the 2kHz communication signal from the power signal.

The external circuits, shown in Figure 4, are required for the ASK demodulation in PeerPower mode. If the user application does not require PeerPower mode, the circuit is not necessary, so connect the DMODIN pin to GND.

The IC can demodulate the PMA advertising packet and WPC FSK with the FSK demodulation block.

The IC demodulates WPC FSK by using positive (+) polarity with modulation depth 0 following WPC Power Class 0 specification, version 1.2.1.

### Foreign Object Detection (FOD)

As stated in the WPC specifications, a foreign object is defined as any object positioned on the interface surface of a base station but not part of the mobile device, such as coins, keys, or other metals. If the foreign object is within the active area, it may heat up during the power transfer, due to eddy currents, resulting from the oscillating magnetic field. Power loss is the key to detecting foreign objects and limiting the power loss on a wireless power system actually limits the heat. To start a power-transfer cycle during the selection phase, the transmitter detects and locates objects that are placed on the interface surface and attempts to differentiate between the foreign objects and a possible power receiver device. Once the wireless power receiver is discovered and the power transmitter completes the identification and the configuration phase, the power receiver reports to the power transmitter its received power in a received power packet ( $P_{RECEIVED}$ ).

The received power ( $P_{PR}$ ) equals the power available from the output of the power receiver, plus any power lost in producing that output power. For example, the power loss includes, but is not limited to:

- Power loss in the secondary coil and series resonant capacitor
- Power loss in the shielding of the power receiver
- Power loss in the rectifier
- Power loss in any post-regulation stage
- Eddy current loss in metal components or contacts within the power receiver

The IC complies with the WPC low-power (v1.2) requirement:

$$P_{RECEIVED} - 350\text{mW} \leq P_{PR} \leq P_{RECEIVED}$$

This means that the reported received power is an over-estimate of the actual received power, by 350mW, where  $P_{PR}$  is the actual received power determined by the mobile device by measuring its load power and adding the estimated parasitic power losses.

The IC has high-precision output current-sensing capabilities and accurate  $V_{RECT}$  control over the operating load, ensuring they are sufficient to estimate the received power and comply with WPC (v1.2) FOD requirements.

The IC provides registers that are  $FOD\_X_n$  and  $FOD\_Y_n$  as part of the received power look-up table (LUT). Based on this LUT, the state machine sends a received power packet that is specified in the WPC requirements.

$FOD\_X_n$  stores 16 X-coordinates for output current values and  $FOD\_Y_n$  stores 16 Y-coordinates of received power values so it makes 16 pairs of coordinates, as shown in [Figure 5](#).

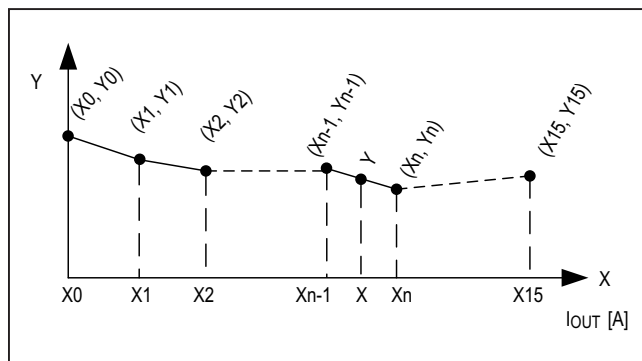


Figure 5. FOD Coefficients vs. Load Current

Between each coordinate, the values are interpolated linearly, as shown in the following equation:

$$y = y_{n-1} + \frac{(x - x_{n-1})(y_n - y_{n-1})}{x_n - x_{n-1}}$$

Equations for the FOD register are:

$$FOD\_X_n = \frac{X_n(A) \times 255 \times 0.73}{1.25}$$

$$FOD\_Y_n = \frac{Y_n(W) \times 128 \times 2}{10}$$

### Watchdog Function

The IC supports a watchdog function that disables the main LDO output in case the watchdog timer expires. When the  $WDOG\_INT\_EN$  bit is set, it enables the watchdog function as well as the associated interrupt ( $WDOG\_INT$ ). The default timer is 41.5s. To keep the main LDO outputs after setting the  $WDOG\_INT\_EN$  bit, an application processor must periodically set the  $WDOG\_INT\_CLR$  bit before the timer expires. If the  $WDOG\_INT\_CLR$  bit is set, the timer is reset, and the  $WDOG\_INT$  bit cleared. This feature prevents the IC from supplying power to a charger when the application processor freezes. To turn the main LDO back on, the application processor needs to set the  $WDOG\_INT\_CLR$  and  $Toggle\_LDO$  bits. The timer options are programmable by OTP.

### Sending End Power Transfer (EPT)/End of Charge (EOC)

The WPC EPT packet and the PMA EOC symbol is sent to a transmitter only by setting  $SEND\_EPT$  bit 1 in  $RX\_COM$  register (address : 0x20) or pulling the DIS pin high. The IC state machine does not send EPT or EOC by itself.

### Sending Proprietary Packets (PPP)

The IC supports PPP, that is defined in the WPC specifications. The maximum length of a PPP is 5 bytes of messages. An example procedure for sending a PPP (3 bytes of messages) is as follows:

1. Write 0x38 in  $PPP\_HEADER[7:0]$
2. Write the first message in  $RX\_DATA\_VALUE0[7:0]$
3. Write the second message in  $RX\_DATA\_VALUE1[7:0]$
4. Write the third message in  $RX\_DATA\_VALUE2[7:0]$
5. Set  $SEND\_RX\_DATA$  bit in  $RX\_COM[7:0]$

## Register Map

| ADDRESS    | NAME                | MSB                |                 |               |                  |                 |                        |                        | LSB                  |
|------------|---------------------|--------------------|-----------------|---------------|------------------|-----------------|------------------------|------------------------|----------------------|
| FUNCTIONAL |                     |                    |                 |               |                  |                 |                        |                        |                      |
| 0x00       | CHIP_ID[7:0]        | CHIP_ID[7:0]       |                 |               |                  |                 |                        |                        |                      |
| 0x05       | OTP_REV[7:0]        | OTP_REV[7:0]       |                 |               |                  |                 |                        |                        |                      |
| 0x06       | STATUS_L[7:0]       | STAT_VOUT          | STAT_VRECT      | STAT_WDOG     | FSK_RCVD         | RESERVED        | RESERVED               | OVER_VOLTAGE           | OVER_CURRENT         |
| 0x07       | STATUS_H[7:0]       | OVER_TEMP          | TX_OVER_CURRENT | TX_OVER_TEMP  | RESERVED         | TX_CONN         | ASK_DEMOD_PING         | ASK_DEMOD_IDCF         | ASK_DEMOD_PT         |
| 0x08       | INT_L[7:0]          | VOUT_INT           | VRECT_INT       | WDOG_INT      | FSK_RCVD_INT     | RESERVED        | RESERVED               | OV_INT                 | OC_INT               |
| 0x09       | INT_H[7:0]          | OT_INT             | TX_OC_INT       | TX_OT_INT     | RESERVED         | TX_CONN_INT     | ASK_DEMOD_PING_INT     | ASK_DEMOD_IDCF_INT     | ASK_DEMOD_PT_INT     |
| 0x0A       | INT_ENABLE_L[7:0]   | VOUT_INT_EN        | VRECT_INT_EN    | WDOG_INT_EN   | FSK_RCVD_INT_EN  | RESERVED        | RESERVED               | OV_INT_EN              | OC_INT_EN            |
| 0x0B       | INT_ENABLE_H[7:0]   | OT_INT_EN          | TX_OC_INT_EN    | TX_OT_INT_EN  | RESERVED         | TX_CONN_INT_EN  | ASK_DEMOD_PING_INT_EN  | ASK_DEMOD_IDCF_INT_EN  | ASK_DEMOD_PT_INT_EN  |
| 0x0C       | INT_CLEAR_L[7:0]    | VOUT_INT_CLR       | VRECT_INT_CLR   | WDOG_INT_CLR  | FSK_RCVD_INT_CLR | RESERVED        | RESERVED               | OV_INT_CLR             | OC_INT_CLR           |
| 0x0D       | INT_CLEAR_H[7:0]    | OT_INT_CLR         | TX_OC_INT_CLR   | TX_OT_INT_CLR | RESERVED         | TX_CONN_INT_CLR | ASK_DEMOD_PING_INT_CLR | ASK_DEMOD_IDCF_INT_CLR | ASK_DEMOD_PT_INT_CLR |
| 0x0E       | CHARGE_STATUS[7:0]  | CHARGE_STATUS[7:0] |                 |               |                  |                 |                        |                        |                      |
| 0x0F       | EPT_REASON[7:0]     | EPT_REASON[7:0]    |                 |               |                  |                 |                        |                        |                      |
| 0x10       | VOUTVAL_H[7:0]      | VOUTVAL[11:4]      |                 |               |                  |                 |                        |                        |                      |
| 0x11       | VOUTVAL_L[7:0]      | RESERVED[3:0]      |                 |               |                  | VOUTVAL[3:0]    |                        |                        |                      |
| 0x12       | VOUTSET[7:0]        | RE-SERVED          | VOUTSET[6:0]    |               |                  |                 |                        |                        |                      |
| 0x13       | VRECT_ADJ[7:0]      | VRECT_ADJ[7:0]     |                 |               |                  |                 |                        |                        |                      |
| 0x14       | VRECTVAL_H[7:0]     | VRECTVAL[11:4]     |                 |               |                  |                 |                        |                        |                      |
| 0x15       | VRECTVAL_L[7:0]     | RESERVED[3:0]      |                 |               |                  | VRECTVAL[3:0]   |                        |                        |                      |
| 0x16       | ISENSEVAL_H[7:0]    | ISENSEVAL[11:4]    |                 |               |                  |                 |                        |                        |                      |
| 0x17       | ISENSEVAL_L[7:0]    | RESERVED[3:0]      |                 |               |                  | ISENSEVAL[3:0]  |                        |                        |                      |
| 0x18       | TDIE_VALUE[7:0]     | TDIE_VALUE[7:0]    |                 |               |                  |                 |                        |                        |                      |
| 0x19       | OP_FREQ_L[7:0]      | OP_FREQ[7:0]       |                 |               |                  |                 |                        |                        |                      |
| 0x1A       | OP_FREQ_H[7:0]      | OP_FREQ[15:8]      |                 |               |                  |                 |                        |                        |                      |
| 0x1B       | PING_OP_FREQ_L[7:0] | PING_OP_FREQ[7:0]  |                 |               |                  |                 |                        |                        |                      |

## Register Map (continued)

| ADDRESS | NAME                  | MSB                  |           |                 |                    |          |           |            | LSB               |
|---------|-----------------------|----------------------|-----------|-----------------|--------------------|----------|-----------|------------|-------------------|
| 0x1C    | PING_OP_FREQ_H[7:0]   | PING_OP_FREQ[15:8]   |           |                 |                    |          |           |            |                   |
| 0x1D    | LDO_ILIMSET[7:0]      | RESERVED[2:0]        |           |                 | LDO_ILIMSET[4:0]   |          |           |            |                   |
| 0x1E    | TX_ILIMSET[7:0]       | RESERVED[2:0]        |           |                 | TX_ILIMSET[4:0]    |          |           |            |                   |
| 0x1F    | SYS_OP_MODE[7:0]      | SYS_OP_MODE[7:0]     |           |                 |                    |          |           |            |                   |
| 0x20    | RX_COM[7:0]           | RE-SERVED            | RE-SERVED | CLEAR_INTERRUPT | SEND_CHARGE_STATUS | SEND_EPT | RE-SERVED | TOGGLE_LDO | SEND_RX_DATA      |
| 0x21    | PPP_HEADER[7:0]       | PPP_HEADER[7:0]      |           |                 |                    |          |           |            |                   |
| 0x22    | RX_DATA_VAL-UE0[7:0]  | RX_DATA_VALUE0[7:0]  |           |                 |                    |          |           |            |                   |
| 0x23    | RX_DATA_VAL-UE1[7:0]  | RX_DATA_VALUE1[7:0]  |           |                 |                    |          |           |            |                   |
| 0x24    | RX_DATA_VAL-UE2[7:0]  | RX_DATA_VALUE2[7:0]  |           |                 |                    |          |           |            |                   |
| 0x25    | RX_DATA_VAL-UE3[7:0]  | RX_DATA_VALUE3[7:0]  |           |                 |                    |          |           |            |                   |
| 0x26    | RX_DATA_VAL-UE4[7:0]  | RX_DATA_VALUE4[7:0]  |           |                 |                    |          |           |            |                   |
| 0x27    | FSK_DATA_VAL-UE0[7:0] | FSK_DATA_VALUE0[7:0] |           |                 |                    |          |           |            |                   |
| 0x28    | FSK_DATA_VAL-UE1[7:0] | FSK_DATA_VALUE1[7:0] |           |                 |                    |          |           |            |                   |
| 0x29    | FSK_DATA_VAL-UE2[7:0] | FSK_DATA_VALUE2[7:0] |           |                 |                    |          |           |            |                   |
| 0x2A    | TX_FOP_SET_L[7:0]     | TX_FOP_SET[7:0]      |           |                 |                    |          |           |            |                   |
| 0x2B    | TX_FOP_SET_H[7:0]     | RESERVED[6:0]        |           |                 |                    |          |           |            | TX_FOP_SET[8]     |
| 0x2C    | TX_FOP_TON_SET_L[7:0] | TX_FOP_TON_SET[7:0]  |           |                 |                    |          |           |            |                   |
| 0x2D    | TX_FOP_TON_SET_H[7:0] | RESERVED[6:0]        |           |                 |                    |          |           |            | TX_FOP_TON_SET[8] |
| 0x34    | TX_WPC_HEADER[7:0]    | TX_WPC_HEADER[7:0]   |           |                 |                    |          |           |            |                   |
| 0x35    | TX_WPC_DATA0[7:0]     | TX_WPC_DATA0[7:0]    |           |                 |                    |          |           |            |                   |
| 0x36    | TX_WPC_DATA1[7:0]     | TX_WPC_DATA1[7:0]    |           |                 |                    |          |           |            |                   |
| 0x37    | TX_WPC_DATA2[7:0]     | TX_WPC_DATA2[7:0]    |           |                 |                    |          |           |            |                   |
| 0x38    | TX_WPC_DATA3[7:0]     | TX_WPC_DATA3[7:0]    |           |                 |                    |          |           |            |                   |
| 0x39    | TX_WPC_DATA4[7:0]     | TX_WPC_DATA4[7:0]    |           |                 |                    |          |           |            |                   |
| 0x3A    | TX_WPC_DATA5[7:0]     | TX_WPC_DATA5[7:0]    |           |                 |                    |          |           |            |                   |
| 0x3B    | TX_WPC_DATA6[7:0]     | TX_WPC_DATA6[7:0]    |           |                 |                    |          |           |            |                   |

## Register Map (continued)

| ADDRESS | NAME                  | MSB                  |  |  |                   |               |  | LSB                   |
|---------|-----------------------|----------------------|--|--|-------------------|---------------|--|-----------------------|
| 0x3C    | TX_WPC_DATA7[7:0]     | TX_WPC_DATA7[7:0]    |  |  |                   |               |  |                       |
| 0x3D    | TX_WPC_CHECKSUM[7:0]  | TX_WPC_CHECKSUM[7:0] |  |  |                   |               |  |                       |
| 0x3E    | FOD_X0[7:0]           | FOD_X0[7:0]          |  |  |                   |               |  |                       |
| 0x3F    | FOD_Y0[7:0]           | FOD_Y0[7:0]          |  |  |                   |               |  |                       |
| 0x40    | FOD_X1[7:0]           | FOD_X1[7:0]          |  |  |                   |               |  |                       |
| 0x41    | FOD_Y1[7:0]           | FOD_Y1[7:0]          |  |  |                   |               |  |                       |
| 0x42    | FOD_X2[7:0]           | FOD_X2[7:0]          |  |  |                   |               |  |                       |
| 0x43    | FOD_Y2[7:0]           | FOD_Y2[7:0]          |  |  |                   |               |  |                       |
| 0x44    | FOD_X3[7:0]           | FOD_X3[7:0]          |  |  |                   |               |  |                       |
| 0x45    | FOD_Y3[7:0]           | FOD_Y3[7:0]          |  |  |                   |               |  |                       |
| 0x46    | FOD_X4[7:0]           | FOD_X4[7:0]          |  |  |                   |               |  |                       |
| 0x47    | FOD_Y4[7:0]           | FOD_Y4[7:0]          |  |  |                   |               |  |                       |
| 0x48    | FOD_X5[7:0]           | FOD_X5[7:0]          |  |  |                   |               |  |                       |
| 0x49    | FOD_Y5[7:0]           | FOD_Y5[7:0]          |  |  |                   |               |  |                       |
| 0x4A    | FOD_X6[7:0]           | FOD_X6[7:0]          |  |  |                   |               |  |                       |
| 0x4B    | FOD_Y6[7:0]           | FOD_Y6[7:0]          |  |  |                   |               |  |                       |
| 0x4C    | FOD_X7[7:0]           | FOD_X7[7:0]          |  |  |                   |               |  |                       |
| 0x4D    | FOD_Y7[7:0]           | FOD_Y7[7:0]          |  |  |                   |               |  |                       |
| 0x4E    | FOD_X8[7:0]           | FOD_X8[7:0]          |  |  |                   |               |  |                       |
| 0x4F    | FOD_Y8[7:0]           | FOD_Y8[7:0]          |  |  |                   |               |  |                       |
| 0x50    | FOD_X9[7:0]           | FOD_X9[7:0]          |  |  |                   |               |  |                       |
| 0x51    | FOD_Y9[7:0]           | FOD_Y9[7:0]          |  |  |                   |               |  |                       |
| 0x52    | FOD_X10[7:0]          | FOD_X10[7:0]         |  |  |                   |               |  |                       |
| 0x53    | FOD_Y10[7:0]          | FOD_Y10[7:0]         |  |  |                   |               |  |                       |
| 0x54    | FOD_X11[7:0]          | FOD_X11[7:0]         |  |  |                   |               |  |                       |
| 0x55    | FOD_Y11[7:0]          | FOD_Y11[7:0]         |  |  |                   |               |  |                       |
| 0x56    | FOD_X12[7:0]          | FOD_X12[7:0]         |  |  |                   |               |  |                       |
| 0x57    | FOD_Y12[7:0]          | FOD_Y12[7:0]         |  |  |                   |               |  |                       |
| 0x58    | FOD_X13[7:0]          | FOD_X13[7:0]         |  |  |                   |               |  |                       |
| 0x59    | FOD_Y13[7:0]          | FOD_Y13[7:0]         |  |  |                   |               |  |                       |
| 0x5A    | FOD_X14[7:0]          | FOD_X14[7:0]         |  |  |                   |               |  |                       |
| 0x5B    | FOD_Y14[7:0]          | FOD_Y14[7:0]         |  |  |                   |               |  |                       |
| 0x5C    | FOD_X15[7:0]          | FOD_X15[7:0]         |  |  |                   |               |  |                       |
| 0x5D    | FOD_Y15[7:0]          | FOD_Y15[7:0]         |  |  |                   |               |  |                       |
| 0x62    | OV_CLAMP_VOLTAGE[7:0] | RESERVED[2:0]        |  |  | POV_CLAMP_VOLTAGE | RESERVED[1:0] |  | OV_CLAMP_VOLTAGE[1:0] |
| 0x63    | TX_LAST_CEP[7:0]      | TX_LAST_CEP[7:0]     |  |  |                   |               |  |                       |

## Register Map (continued)

| ADDRESS      | NAME                     | MSB                      |                       |                        |                        |  |  | LSB |
|--------------|--------------------------|--------------------------|-----------------------|------------------------|------------------------|--|--|-----|
| 0x64         | TX_LAST_RPP[7:0]         | TX_LAST_RPP[7:0]         |                       |                        |                        |  |  |     |
| 0x65         | TX_LAST_PCHP[7:0]        | TX_LAST_PCHP[7:0]        |                       |                        |                        |  |  |     |
| LDO          |                          |                          |                       |                        |                        |  |  |     |
| 0x70         | LDO_WPDET_CNFG[7:0]      | WPDET_H_DEBOUNCE[1:0]    | WPDET_L_DEBOUNCE[1:0] | WPDET_H_THRESHOLD[1:0] | WPDET_L_THRESHOLD[1:0] |  |  |     |
| VRECT_TARGET |                          |                          |                       |                        |                        |  |  |     |
| 0xBA         | VRECT_TARGET_X0[7:0]     | VRECT_TARGET_X0[7:0]     |                       |                        |                        |  |  |     |
| 0xBB         | VRECT_TARGET_Y0[7:0]     | VRECT_TARGET_Y0[7:0]     |                       |                        |                        |  |  |     |
| 0xBC         | VRECT_TARGET_PMA_Y0[7:0] | VRECT_TARGET_PMA_Y0[7:0] |                       |                        |                        |  |  |     |
| 0xBD         | VRECT_TARGET_X1[7:0]     | VRECT_TARGET_X1[7:0]     |                       |                        |                        |  |  |     |
| 0xBE         | VRECT_TARGET_Y1[7:0]     | VRECT_TARGET_Y1[7:0]     |                       |                        |                        |  |  |     |
| 0xBF         | VRECT_TARGET_PMA_Y1[7:0] | VRECT_TARGET_PMA_Y1[7:0] |                       |                        |                        |  |  |     |
| 0xC0         | VRECT_TARGET_X2[7:0]     | VRECT_TARGET_X2[7:0]     |                       |                        |                        |  |  |     |
| 0xC1         | VRECT_TARGET_Y2[7:0]     | VRECT_TARGET_Y2[7:0]     |                       |                        |                        |  |  |     |
| 0xC2         | VRECT_TARGET_PMA_Y2[7:0] | VRECT_TARGET_PMA_Y2[7:0] |                       |                        |                        |  |  |     |
| 0xC3         | VRECT_TARGET_X3[7:0]     | VRECT_TARGET_X3[7:0]     |                       |                        |                        |  |  |     |
| 0xC4         | VRECT_TARGET_Y3[7:0]     | VRECT_TARGET_Y3[7:0]     |                       |                        |                        |  |  |     |
| 0xC5         | VRECT_TARGET_PMA_Y3[7:0] | VRECT_TARGET_PMA_Y3[7:0] |                       |                        |                        |  |  |     |
| 0xC6         | VRECT_TARGET_X4[7:0]     | VRECT_TARGET_X4[7:0]     |                       |                        |                        |  |  |     |
| 0xC7         | VRECT_TARGET_Y4[7:0]     | VRECT_TARGET_Y4[7:0]     |                       |                        |                        |  |  |     |
| 0xC8         | VRECT_TARGET_PMA_Y4[7:0] | VRECT_TARGET_PMA_Y4[7:0] |                       |                        |                        |  |  |     |
| 0xC9         | VRECT_TARGET_X5[7:0]     | VRECT_TARGET_X5[7:0]     |                       |                        |                        |  |  |     |
| 0xCA         | VRECT_TARGET_Y5[7:0]     | VRECT_TARGET_Y5[7:0]     |                       |                        |                        |  |  |     |
| 0xCB         | VRECT_TARGET_PMA_Y5[7:0] | VRECT_TARGET_PMA_Y5[7:0] |                       |                        |                        |  |  |     |

## Register Map (continued)

| ADDRESS | NAME                     | MSB                      |  |  |  |                  |  | LSB |
|---------|--------------------------|--------------------------|--|--|--|------------------|--|-----|
| 0xCC    | VRECT_TARGET_X6[7:0]     | VRECT_TARGET_X6[7:0]     |  |  |  |                  |  |     |
| 0xCD    | VRECT_TARGET_Y6[7:0]     | VRECT_TARGET_Y6[7:0]     |  |  |  |                  |  |     |
| 0xCE    | VRECT_TARGET_PMA_Y6[7:0] | VRECT_TARGET_PMA_Y6[7:0] |  |  |  |                  |  |     |
| 0xCF    | VRECT_TARGET_X7[7:0]     | VRECT_TARGET_X7[7:0]     |  |  |  |                  |  |     |
| 0xD0    | VRECT_TARGET_Y7[7:0]     | VRECT_TARGET_Y7[7:0]     |  |  |  |                  |  |     |
| 0xD1    | VRECT_TARGET_PMA_Y7[7:0] | VRECT_TARGET_PMA_Y7[7:0] |  |  |  |                  |  |     |
| DEMOD   |                          |                          |  |  |  |                  |  |     |
| 0xDB    | PMA_ADV_DATA[7:0]        | PMA_ADV_DATA[7:0]        |  |  |  |                  |  |     |
| 0xDC    | PMA_ADV_CRC[7:0]         | RESERVED[3:0]            |  |  |  | PMA_ADV_CRC[3:0] |  |     |

## CHIP\_ID (0x00)

| BIT         | 7            | 6    | 5 | 4           | 3 | 2 | 1 | 0 |
|-------------|--------------|------|---|-------------|---|---|---|---|
| Field       | CHIP_ID[7:0] |      |   |             |   |   |   |   |
| Reset       | 0b0001_0010  |      |   |             |   |   |   |   |
| Access Type | Read Only    |      |   |             |   |   |   |   |
| BITFIELD    |              | BITS |   | DESCRIPTION |   |   |   |   |
| CHIP_ID     |              | 7:0  |   | -           |   |   |   |   |

## OTP\_REV (0x05)

| BIT         | 7            | 6    | 5 | 4            | 3 | 2 | 1 | 0 |
|-------------|--------------|------|---|--------------|---|---|---|---|
| Field       | OTP_REV[7:0] |      |   |              |   |   |   |   |
| Reset       | 0b0000_0000  |      |   |              |   |   |   |   |
| Access Type | Read Only    |      |   |              |   |   |   |   |
| BITFIELD    |              | BITS |   | DESCRIPTION  |   |   |   |   |
| OTP_REV     |              | 7:0  |   | OTP revision |   |   |   |   |

**STATUS\_L (0x06)**

| BIT         | 7         | 6          | 5         | 4         | 3         | 2         | 1            | 0            |
|-------------|-----------|------------|-----------|-----------|-----------|-----------|--------------|--------------|
| Field       | STAT_VOUT | STAT_VRECT | STAT_WDOG | FSK_RCVD  | RESERVED  | RESERVED  | OVER_VOLTAGE | OVER_CURRENT |
| Reset       | 0b0       | 0b0        | 0b0       | 0b0       | 0b0       | 0b0       | 0b0          | 0b0          |
| Access Type | Read Only | Read Only  | Read Only | Read Only | Read Only | Read Only | Read Only    | Read Only    |

| BITFIELD     | BITS | DESCRIPTION                                                   |
|--------------|------|---------------------------------------------------------------|
| STAT_VOUT    | 7    | 1: LDO is ON<br>0: LDO is OFF (Rx ONLY)                       |
| STAT_VRECT   | 6    | 1: VRECT is over UVLO (Rx ONLY)                               |
| STAT_WDOG    | 5    | 1: Watchdog timer expires<br>0: No watchdog timer expires     |
| FSK_RCVD     | 4    | 1: FSK data sent by transmitter is received<br>0: No FSK data |
| RESERVED     | 3    | RSVD                                                          |
| RESERVED     | 2    | RSVD                                                          |
| OVER_VOLTAGE | 1    | 1: Overvoltage (VRECT)<br>0: Normal                           |
| OVER_CURRENT | 0    | 1: Overcurrent (LDO output current) in Rx mode<br>0: Normal   |

**STATUS\_H (0x07)**

| BIT         | 7         | 6               | 5            | 4         | 3         | 2              | 1              | 0            |
|-------------|-----------|-----------------|--------------|-----------|-----------|----------------|----------------|--------------|
| Field       | OVER_TEMP | TX_OVER_CURRENT | TX_OVER_TEMP | RESERVED  | TX_CONN   | ASK_DEMOD_PING | ASK_DEMOD_IDCF | ASK_DEMOD_PT |
| Reset       | 0b0       | 0b0             | 0b0          | 0b0       | 0b0       | 0b0            | 0b0            | 0b0          |
| Access Type | Read Only | Read Only       | Read Only    | Read Only | Read Only | Read Only      | Read Only      | Read Only    |

| BITFIELD        | BITS | DESCRIPTION                                                                                |
|-----------------|------|--------------------------------------------------------------------------------------------|
| OVER_TEMP       | 7    | 1: Overtemperature in Rx mode<br>0: Normal                                                 |
| TX_OVER_CURRENT | 6    | 1: Overcurrent in Tx mode<br>0: Normal                                                     |
| TX_OVER_TEMP    | 5    | 1: Overtemperature in Tx mode<br>0: Normal                                                 |
| RESERVED        | 4    | RSVD                                                                                       |
| TX_CONN         | 3    | 1: Power transfer established in Tx mode<br>0: No power transfer established               |
| ASK_DEMOD_PING  | 2    | 1: Packet received in PING phase<br>0: No packet                                           |
| ASK_DEMOD_IDCF  | 1    | 1: Packet received in ID and configuration phase<br>0: No packet                           |
| ASK_DEMOD_PT    | 0    | 1: Packet received in power transfer phase (count CEP if that is non zero)<br>0: No packet |



**INT\_L (0x08)**

| BIT         | 7         | 6         | 5         | 4            | 3         | 2         | 1         | 0         |
|-------------|-----------|-----------|-----------|--------------|-----------|-----------|-----------|-----------|
| Field       | VOUT_INT  | VRECT_INT | WDOG_INT  | FSK_RCVD_INT | RESERVED  | RESERVED  | OV_INT    | OC_INT    |
| Reset       | 0b0       | 0b0       | 0b0       | 0b0          | 0b0       | 0b0       | 0b0       | 0b0       |
| Access Type | Read Only | Read Only | Read Only | Read Only    | Read Only | Read Only | Read Only | Read Only |

| BITFIELD     | BITS | DESCRIPTION                                                 |
|--------------|------|-------------------------------------------------------------|
| VOUT_INT     | 7    | 1: V <sub>OUT</sub> state change (off to on, on to off)     |
| VRECT_INT    | 6    | 1: V <sub>RECT</sub> is over UVLO (Rx ONLY)                 |
| WDOG_INT     | 5    | 1: Watchdog timer expired                                   |
| FSK_RCVD_INT | 4    | 1: FSK data sent by transmitter is received                 |
| RESERVED     | 3    | RSVD                                                        |
| RESERVED     | 2    | RSVD                                                        |
| OV_INT       | 1    | 1: Overvoltage (V <sub>RECT</sub> )<br>0: Normal            |
| OC_INT       | 0    | 1: Overcurrent (LDO output current) in Rx mode<br>0: Normal |

**INT\_H (0x09)**

| BIT         | 7         | 6         | 5         | 4         | 3           | 2                  | 1                  | 0                |
|-------------|-----------|-----------|-----------|-----------|-------------|--------------------|--------------------|------------------|
| Field       | OT_INT    | TX_OC_INT | TX_OT_INT | RESERVED  | TX_CONN_INT | ASK_DEMOD_PING_INT | ASK_DEMOD_IDCF_INT | ASK_DEMOD_PT_INT |
| Reset       | 0b0       | 0b0       | 0b0       | 0b0       | 0b0         | 0b0                | 0b0                | 0b0              |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only   | Read Only          | Read Only          | Read Only        |

| BITFIELD           | BITS | DESCRIPTION                                      |
|--------------------|------|--------------------------------------------------|
| OT_INT             | 7    | 1: Overtemperature in Rx mode                    |
| TX_OC_INT          | 6    | 1: Overcurrent in Tx mode                        |
| TX_OT_INT          | 5    | 1: Overtemperature in Tx mode                    |
| RESERVED           | 4    | RSVD                                             |
| TX_CONN_INT        | 3    | 1: Power tranfer phase established in Tx mode    |
| ASK_DEMOD_PING_INT | 2    | 1: Packet received in PING Phase                 |
| ASK_DEMOD_IDCF_INT | 1    | 1: Packet received in ID and configuration phase |
| ASK_DEMOD_PT_INT   | 0    | 1: Packet received in power transfer phase       |

**INT\_ENABLE\_L (0x0A)**

| BIT         | 7           | 6            | 5           | 4               | 3           | 2           | 1           | 0           |
|-------------|-------------|--------------|-------------|-----------------|-------------|-------------|-------------|-------------|
| Field       | VOUT_INT_EN | VRECT_INT_EN | WDOG_INT_EN | FSK_RCVD_INT_EN | RESERVED    | RESERVED    | OV_INT_EN   | OC_INT_EN   |
| Reset       | 0b0         | 0b0          | 0b0         | 0b0             | 0b0         | 0b0         | 0b0         | 0b0         |
| Access Type | Write, Read | Write, Read  | Write, Read | Write, Read     | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD        | BITS | DESCRIPTION                                                     |
|-----------------|------|-----------------------------------------------------------------|
| VOUT_INT_EN     | 7    | 1: Enable VOUT_INT<br>0: Disable                                |
| VRECT_INT_EN    | 6    | 1: Enable VRECT_INT<br>0: Disable                               |
| WDOG_INT_EN     | 5    | 1: Enable watchdog timer and associated interrupt<br>0: Disable |
| FSK_RCVD_INT_EN | 4    | 1: Enable FSK_RCVD_INT<br>0: Disable                            |
| RESERVED        | 3    | RSVD                                                            |
| RESERVED        | 2    | RSVD                                                            |
| OV_INT_EN       | 1    | 1: Enable OV_INT<br>0: Disable                                  |
| OC_INT_EN       | 0    | 1: Enable OC_INT<br>0: Disable                                  |

**INT\_ENABLE\_H (0x0B)**

| BIT         | 7           | 6            | 5            | 4           | 3              | 2                     | 1                     | 0                   |
|-------------|-------------|--------------|--------------|-------------|----------------|-----------------------|-----------------------|---------------------|
| Field       | OT_INT_EN   | TX_OC_INT_EN | TX_OT_INT_EN | RESERVED    | TX_CONN_INT_EN | ASK_DEMOD_PING_INT_EN | ASK_DEMOD_IDCF_INT_EN | ASK_DEMOD_PT_INT_EN |
| Reset       | 0b0         | 0b0          | 0b0          | 0b0         | 0b0            | 0b0                   | 0b0                   | 0b0                 |
| Access Type | Write, Read | Write, Read  | Write, Read  | Write, Read | Write, Read    | Write, Read           | Write, Read           | Write, Read         |

| BITFIELD              | BITS | DESCRIPTION                                |
|-----------------------|------|--------------------------------------------|
| OT_INT_EN             | 7    | 1: Enable OT_INT<br>0: Disable             |
| TX_OC_INT_EN          | 6    | 1: Enable TX_OC_INT<br>0: Disable          |
| TX_OT_INT_EN          | 5    | 1: Enable TX_OT_INT<br>0: Disable          |
| RESERVED              | 4    | RSVD                                       |
| TX_CONN_INT_EN        | 3    | 1: Enable TX_CONN_INT<br>0: Disable        |
| ASK_DEMOD_PING_INT_EN | 2    | 1: Enable ASK_DEMOD_PING_INT<br>0: Disable |
| ASK_DEMOD_IDCF_INT_EN | 1    | 1: Enable ASK_DEMOD_IDCF_INT<br>0: Disable |
| ASK_DEMOD_PT_INT_EN   | 0    | 1: Enable ASK_DEMOD_PT_INT<br>0: Disable   |

**INT\_CLEAR\_L (0x0C)**

| BIT         | 7            | 6             | 5            | 4                | 3           | 2           | 1           | 0           |
|-------------|--------------|---------------|--------------|------------------|-------------|-------------|-------------|-------------|
| Field       | VOUT_INT_CLR | VRECT_INT_CLR | WDOG_INT_CLR | FSK_RCVD_INT_CLR | RESERVED    | RESERVED    | OV_INT_CLR  | OC_INT_CLR  |
| Reset       | 0b0          | 0b0           | 0b0          | 0b0              | 0b0         | 0b0         | 0b0         | 0b0         |
| Access Type | Write, Read  | Write, Read   | Write, Read  | Write, Read      | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD         | BITS | DESCRIPTION                                                                |
|------------------|------|----------------------------------------------------------------------------|
| VOUT_INT_CLR     | 7    | 1: Clear VOUT_INT bit (this CLR bit resets automatically after being set)  |
| VRECT_INT_CLR    | 6    | 1: Clear VRECT_INT bit (this CLR bit resets automatically after being set) |
| WDOG_INT_CLR     | 5    | 1: Clear WDOG_INT bit (this CLR bit resets automatically after being set)  |
| FSK_RCVD_INT_CLR | 4    | 1: Clear FSK_RCVD_INT (this CLR bit resets automatically after being set)  |
| RESERVED         | 3    | RSVD                                                                       |
| RESERVED         | 2    | RSVD                                                                       |
| OV_INT_CLR       | 1    | 1: Clear OV_INT bit (this CLR bit resets automatically after being set)    |
| OC_INT_CLR       | 0    | 1: Clear OC_INT bit (this CLR bit resets automatically after being set)    |

**INT\_CLEAR\_H (0x0D)**

| BIT         | 7           | 6             | 5             | 4           | 3               | 2                      | 1                      | 0                    |
|-------------|-------------|---------------|---------------|-------------|-----------------|------------------------|------------------------|----------------------|
| Field       | OT_INT_CLR  | TX_OC_INT_CLR | TX_OT_INT_CLR | RESERVED    | TX_CONN_INT_CLR | ASK_DEMOD_PING_INT_CLR | ASK_DEMOD_IDCF_INT_CLR | ASK_DEMOD_PT_INT_CLR |
| Reset       | 0b0         | 0b0           | 0b0           | 0b0         | 0b0             | 0b0                    | 0b0                    | 0b0                  |
| Access Type | Write, Read | Write, Read   | Write, Read   | Write, Read | Write, Read     | Write, Read            | Write, Read            | Write, Read          |

| BITFIELD               | BITS | DESCRIPTION                                                                         |
|------------------------|------|-------------------------------------------------------------------------------------|
| OT_INT_CLR             | 7    | 1: Clear OT_INT bit (this CLR bit resets automatically after being set)             |
| TX_OC_INT_CLR          | 6    | 1: Clear TX_OC_INT bit (this CLR bit resets automatically after being set)          |
| TX_OT_INT_CLR          | 5    | 1: Clear TX_OT_INT bit (this CLR bit resets automatically after being set)          |
| RESERVED               | 4    | RSVD                                                                                |
| TX_CONN_INT_CLR        | 3    | 1: Clear TX_CONN_INT bit (this CLR bit resets automatically after being set)        |
| ASK_DEMOD_PING_INT_CLR | 2    | 1: Clear ASK_DEMOD_PING_INT bit (this CLR bit resets automatically after being set) |
| ASK_DEMOD_IDCF_INT_CLR | 1    | 1: Clear ASK_DEMOD_IDCF_INT bit (this CLR bit resets automatically after being set) |
| ASK_DEMOD_PT_INT_CLR   | 0    | 1: Clear ASK_DEMOD_PT_INT bit (this CLR bit resets automatically after being set)   |

**CHARGE\_STATUS (0x0E)**

| BIT         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field       | CHARGE_STATUS[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1111_1111        |   |   |   |   |   |   |   |
| Access Type | Write, Read        |   |   |   |   |   |   |   |

| BITFIELD      | BITS | DESCRIPTION                                                                                                                                                                                                                                                                    |
|---------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CHARGE_STATUS | 7:0  | Register for storing charge status as follows:<br>0x00: Reserved<br>0x01: Charge status = 1 (1%)<br>0x02: Charge status = 2 (2%)<br>.....<br>0x64: Charge status = 64 (100%)<br>0x65 to 0xFE: Reserved<br>0xFF: No battery charge device or not providing charge status packet |

**EPT\_REASON (0x0F)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | EPT_REASON[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1111_1111     |   |   |   |   |   |   |   |
| Access Type | Write, Read     |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                   |
|------------|------|---------------------------------------------------------------------------------------------------------------|
| EPT_REASON | 7:0  | A user can program the reason for the end power transfer request that is specified in the WPC specifications. |

**VOUTVAL\_H (0x10)**

| BIT         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Field       | VOUTVAL[11:4] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000   |   |   |   |   |   |   |   |
| Access Type | Read Only     |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                              |
|----------|------|------------------------------------------------------------------------------------------|
| VOUTVAL  | 7:0  | 8 MSB of VOUTVAL ADC value.<br>$V_{OUT}(V) = VOUTVAL[11:0] \times (1.25/4095) \times 12$ |

**VOUTVAL\_L (0x11)**

| BIT         | 7             | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
|-------------|---------------|---|---|---|--------------|---|---|---|
| Field       | RESERVED[3:0] |   |   |   | VOUTVAL[3:0] |   |   |   |
| Reset       | 0b0000        |   |   |   | 0b0000       |   |   |   |
| Access Type | Read Only     |   |   |   | Read Only    |   |   |   |

| BITFIELD | BITS | DESCRIPTION                |
|----------|------|----------------------------|
| RESERVED | 7:4  | RSVD                       |
| VOUTVAL  | 3:0  | 4 LSB of VOUTVAL ADC value |

**VOUTSET (0x12)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | VOUTSET[6:0] |   |   |   |   |   |   |   |
| Reset       | 0b011_0010   |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                         |
|----------|------|-------------------------------------------------------------------------------------|
| RESERVED | 7    | RSVD                                                                                |
| VOUTSET  | 6:0  | Main LDO output-voltage-setting register.<br>$V_{OUT}(V) = VOUTSET[6:0] \times 0.1$ |

**VRECT\_ADJ (0x13)**

| BIT         | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---|---|---|---|---|---|
| Field       | VRECT_ADJ[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000    |   |   |   |   |   |   |   |
| Access Type | Write, Read    |   |   |   |   |   |   |   |

| BITFIELD  | BITS | DESCRIPTION                                                                                                 |
|-----------|------|-------------------------------------------------------------------------------------------------------------|
| VRECT_ADJ | 7:0  | 2's complement signed integer representing values -128 ~ +127.<br>Adjustment(V) = VRECT_ADJ x 12 x 1.25/255 |

**VRECTVAL\_H (0x14)**

| BIT         | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---|---|---|---|---|---|
| Field       | VRECTVAL[11:4] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000    |   |   |   |   |   |   |   |
| Access Type | Read Only      |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                 |
|----------|------|---------------------------------------------------------------------------------------------|
| VRECTVAL | 7:0  | 8 MSB of VRECTVAL ADC value.<br>$V_{RECT}(V) = VRECTVAL[11:0] \times (1.25/4095) \times 12$ |

**VRECTVAL\_L (0x15)**

| BIT         | 7             | 6 | 5 | 4 | 3             | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---------------|---|---|---|
| Field       | RESERVED[3:0] |   |   |   | VRECTVAL[3:0] |   |   |   |
| Reset       | 0b0000        |   |   |   | 0b0000        |   |   |   |
| Access Type | Read Only     |   |   |   | Read Only     |   |   |   |

| BITFIELD | BITS | DESCRIPTION                 |
|----------|------|-----------------------------|
| RESERVED | 7:4  | RSVD                        |
| VRECTVAL | 3:0  | 4 LSB of VRECTVAL ADC value |

**ISENSEVAL\_H (0x16)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | ISENSEVAL[11:4] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000     |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD  | BITS | DESCRIPTION                                                                                                                                 |
|-----------|------|---------------------------------------------------------------------------------------------------------------------------------------------|
| ISENSEVAL | 7:0  | 8 MSB of ISENSE ADC value. $ISENSE(A) = ISENSEVAL[11:0] \times (1.25/4095) \times (1/0.73)$ . Bidirectional measurement for Rx and Tx mode. |

**ISENSEVAL\_L (0x17)**

| BIT         | 7             | 6 | 5 | 4 | 3              | 2 | 1 | 0 |
|-------------|---------------|---|---|---|----------------|---|---|---|
| Field       | RESERVED[3:0] |   |   |   | ISENSEVAL[3:0] |   |   |   |
| Reset       | 0b0000        |   |   |   | 0b0000         |   |   |   |
| Access Type | Read Only     |   |   |   | Read Only      |   |   |   |

| BITFIELD  | BITS | DESCRIPTION                  |
|-----------|------|------------------------------|
| RESERVED  | 7:4  | RSVD                         |
| ISENSEVAL | 3:0  | 4 LSB of ISENSEVAL ADC value |

**TDIE\_VALUE (0x18)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | TDIE_VALUE[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000     |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                        |
|------------|------|------------------------------------------------------------------------------------|
| TDIE_VALUE | 7:0  | Die temperature value = $TDIE\_VALUE[7:0] \times 16 \times 0.108603481 - 262.1459$ |

**OP\_FREQ\_L (0x19)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | OP_FREQ[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000  |   |   |   |   |   |   |   |
| Access Type | Read Only    |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                              |
|----------|------|----------------------------------------------------------------------------------------------------------|
| OP_FREQ  | 7:0  | 8 LSB of OP_FREQ. AC operation frequency in Rx and Tx mode. $FREQ(Hz) = 64 \times 10^6 / OP\_FREQ[15:0]$ |

**OP\_FREQ\_H (0x1A)**

| BIT         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Field       | OP_FREQ[15:8] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000   |   |   |   |   |   |   |   |
| Access Type | Read Only     |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                        |
|----------|------|--------------------------------------------------------------------------------------------------------------------|
| OP_FREQ  | 7:0  | 8 MSB of OP_FREQ. AC operation frequency in Rx and Tx mode.<br>FREQ(Hz) = $64 \times 10^6 / \text{OP\_FREQ}[15:0]$ |

**PING\_OP\_FREQ\_L (0x1B)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | PING_OP_FREQ[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                             |
|--------------|------|-------------------------------------------------------------------------------------------------------------------------|
| PING_OP_FREQ | 7:0  | 8 LSB of PING_OP_FREQ. AC frequency captured in PING phase.<br>PING FREQ(Hz) = $64 \times 10^6 / \text{OP\_FREQ}[15:0]$ |

**PING\_OP\_FREQ\_H (0x1C)**

| BIT         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field       | PING_OP_FREQ[15:8] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000        |   |   |   |   |   |   |   |
| Access Type | Read Only          |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                 |
|--------------|------|-------------------------------------------------------------|
| PING_OP_FREQ | 7:0  | 8 MSB of PING_OP_FREQ. AC frequency captured in PING phase. |

**LDO\_ILIMSET (0x1D)**

| BIT         | 7             | 6 | 5 | 4                | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|------------------|---|---|---|---|
| Field       | RESERVED[2:0] |   |   | LDO_ILIMSET[4:0] |   |   |   |   |
| Reset       | 0b000         |   |   | 0b1_1010         |   |   |   |   |
| Access Type | Write, Read   |   |   | Write, Read      |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                             |
|-------------|------|-------------------------------------------------------------------------------------------------------------------------|
| RESERVED    | 7:5  | RSVD                                                                                                                    |
| LDO_ILIMSET | 4:0  | LDO current-limit-setting register. ILIM(A) = LDO_ILIMSET[4:0] x 0.05. ILIM lower clamp = 20mA, ILIM upper clamp = 1.5A |

**TX\_ILIMSET (0x1E)**

| BIT         | 7             | 6 | 5 | 4               | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|-----------------|---|---|---|---|
| Field       | RESERVED[2:0] |   |   | TX_ILIMSET[4:0] |   |   |   |   |
| Reset       | 0b000         |   |   | 0b0_1010        |   |   |   |   |
| Access Type | Write, Read   |   |   | Write, Read     |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                  |
|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------|
| RESERVED   | 7:5  | RSVD                                                                                                                                         |
| TX_ILIMSET | 4:0  | Tx (PeerPower) mode input current-limit-setting register. ILIM(A) = TX_ILIMSET[4:0] x 0.05. ILIM lower clamp = 20mA, ILIM upper clamp = 1.5A |

**SYS\_OP\_MODE (0x1F)**

| BIT         | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field       | SYS_OP_MODE[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000      |   |   |   |   |   |   |   |
| Access Type | Read Only        |   |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                |
|-------------|------|--------------------------------------------------------------------------------------------|
| SYS_OP_MODE | 7:0  | 0x00: Initial state<br>0x01: WPC Rx mode<br>0x02: PMA Rx mode<br>0x04: Tx mode (PeerPower) |

**RX\_COM (0x20)**

| BIT         | 7           | 6           | 5               | 4                  | 3           | 2           | 1           | 0            |
|-------------|-------------|-------------|-----------------|--------------------|-------------|-------------|-------------|--------------|
| Field       | RESERVED    | RESERVED    | CLEAR_INTERRUPT | SEND_CHARGE_STATUS | SEND_EPT    | RESERVED    | TOGGLE_LDO  | SEND_RX_DATA |
| Reset       | 0b0         | 0b0         | 0b0             | 0b0                | 0b0         | 0b0         | 0b0         | 0b0          |
| Access Type | Write, Read | Write, Read | Write, Read     | Write, Read        | Write, Read | Write, Read | Write, Read | Write, Read  |

| BITFIELD           | BITS | DESCRIPTION                                                                                                                                                  |
|--------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RESERVED           | 7    | RSVD                                                                                                                                                         |
| RESERVED           | 6    | RSVD                                                                                                                                                         |
| CLEAR_INTERRUPT    | 5    | Global Interrupt Clear Bit. Clears all interrupt bits. After the set, it resets automatically.                                                               |
| SEND_CHARGE_STATUS | 4    | 1: Send charge status packet. After the set, it resets automatically.                                                                                        |
| SEND_EPT           | 3    | 1: Send end power transfer packet. After the set, it resets automatically.                                                                                   |
| RESERVED           | 2    | RSVD                                                                                                                                                         |
| TOGGLE_LDO         | 1    | 1: Toggle LDO output once (on to off, off to on). After the set, it resets automatically.                                                                    |
| SEND_RX_DATA       | 0    | 1: Send WPC proprietary packet that includes PPP_Header (0x21), data command (0x22), and data values (0x23 to 0x26). After the set, it resets automatically. |



**PPP\_HEADER (0x21)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | PPP_HEADER[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000     |   |   |   |   |   |   |   |
| Access Type | Write, Read     |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                   |
|------------|------|-------------------------------|
| PPP_HEADER | 7:0  | WPC Proprietary Packet Header |

**RX\_DATA\_VALUE0 (0x22)**

| BIT         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field       | RX_DATA_VALUE0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000         |   |   |   |   |   |   |   |
| Access Type | Write, Read         |   |   |   |   |   |   |   |

| BITFIELD       | BITS | DESCRIPTION                    |
|----------------|------|--------------------------------|
| RX_DATA_VALUE0 | 7:0  | 1st Byte of Proprietary Packet |

**RX\_DATA\_VALUE1 (0x23)**

| BIT         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field       | RX_DATA_VALUE1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000         |   |   |   |   |   |   |   |
| Access Type | Write, Read         |   |   |   |   |   |   |   |

| BITFIELD       | BITS | DESCRIPTION                    |
|----------------|------|--------------------------------|
| RX_DATA_VALUE1 | 7:0  | 2nd Byte of Proprietary Packet |

**RX\_DATA\_VALUE2 (0x24)**

| BIT         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field       | RX_DATA_VALUE2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000         |   |   |   |   |   |   |   |
| Access Type | Write, Read         |   |   |   |   |   |   |   |

| BITFIELD       | BITS | DESCRIPTION                    |
|----------------|------|--------------------------------|
| RX_DATA_VALUE2 | 7:0  | 3rd Byte of Proprietary Packet |

**RX\_DATA\_VALUE3 (0x25)**

| BIT         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field       | RX_DATA_VALUE3[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000         |   |   |   |   |   |   |   |
| Access Type | Write, Read         |   |   |   |   |   |   |   |

| BITFIELD       | BITS | DESCRIPTION                    |
|----------------|------|--------------------------------|
| RX_DATA_VALUE3 | 7:0  | 4th Byte of Proprietary Packet |

**RX\_DATA\_VALUE4 (0x26)**

| BIT         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field       | RX_DATA_VALUE4[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000         |   |   |   |   |   |   |   |
| Access Type | Write, Read         |   |   |   |   |   |   |   |

| BITFIELD       | BITS | DESCRIPTION                    |
|----------------|------|--------------------------------|
| RX_DATA_VALUE4 | 7:0  | 5th Byte of Proprietary Packet |

**FSK\_DATA\_VALUE0 (0x27)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | FSK_DATA_VALUE0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000          |   |   |   |   |   |   |   |
| Access Type | Read Only            |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION          |
|-----------------|------|----------------------|
| FSK_DATA_VALUE0 | 7:0  | 1st Byte of FSK_DATA |

**FSK\_DATA\_VALUE1 (0x28)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | FSK_DATA_VALUE1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000          |   |   |   |   |   |   |   |
| Access Type | Read Only            |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION          |
|-----------------|------|----------------------|
| FSK_DATA_VALUE1 | 7:0  | 2nd Byte of FSK_DATA |

**FSK\_DATA\_VALUE2 (0x29)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | FSK_DATA_VALUE2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000          |   |   |   |   |   |   |   |
| Access Type | Read Only            |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION          |
|-----------------|------|----------------------|
| FSK_DATA_VALUE2 | 7:0  | 3rd Byte of FSK_DATA |

**TX\_FOP\_SET\_L (0x2A)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | TX_FOP_SET[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1111_1111     |   |   |   |   |   |   |   |
| Access Type | Write, Read     |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                    |
|------------|------|--------------------------------------------------------------------------------|
| TX_FOP_SET | 7:0  | Tx operating frequency = $64 \times 10^6 / (2 \times (TX\_FOP\_SET[8:0] + 1))$ |

**TX\_FOP\_SET\_H (0x2B)**

| BIT         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0             |
|-------------|---------------|---|---|---|---|---|---|---------------|
| Field       | RESERVED[6:0] |   |   |   |   |   |   | TX_FOP_SET[8] |
| Reset       | 0b0000_000    |   |   |   |   |   |   | 0b0           |
| Access Type | Write, Read   |   |   |   |   |   |   | Write, Read   |

| BITFIELD   | BITS | DESCRIPTION |
|------------|------|-------------|
| RESERVED   | 7:1  | RSVD        |
| TX_FOP_SET | 0    |             |

**TX\_FOP\_TON\_SET\_L (0x2C)**

| BIT         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field       | TX_FOP_TON_SET[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000         |   |   |   |   |   |   |   |
| Access Type | Write, Read         |   |   |   |   |   |   |   |

| BITFIELD       | BITS | DESCRIPTION                                                                                                 |
|----------------|------|-------------------------------------------------------------------------------------------------------------|
| TX_FOP_TON_SET | 7:0  | $Tx \text{ duty cycle} = (TX\_FOP\_SET[8:0] - TX\_FOP\_TON\_SET[8:0]) / (2 \times (TX\_FOP\_SET[8:0] + 1))$ |

**TX\_FOP\_TON\_SET\_H (0x2D)**

| BIT         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0                 |
|-------------|---------------|---|---|---|---|---|---|-------------------|
| Field       | RESERVED[6:0] |   |   |   |   |   |   | TX_FOP_TON_SET[8] |
| Reset       | 0b0000_000    |   |   |   |   |   |   | 0b0               |
| Access Type | Write, Read   |   |   |   |   |   |   | Write, Read       |

| BITFIELD       | BITS | DESCRIPTION |
|----------------|------|-------------|
| RESERVED       | 7:1  | RSVD        |
| TX_FOP_TON_SET | 0    |             |

**TX\_WPC\_HEADER (0x34)**

| BIT         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_HEADER[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000        |   |   |   |   |   |   |   |
| Access Type | Read Only          |   |   |   |   |   |   |   |

| BITFIELD      | BITS | DESCRIPTION                                                                   |
|---------------|------|-------------------------------------------------------------------------------|
| TX_WPC_HEADER | 7:0  | Header of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA0 (0x35)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA0 | 7:0  | DATA0 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA1 (0x36)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA1 | 7:0  | DATA1 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA2 (0x37)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA2 | 7:0  | DATA2 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA3 (0x38)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA3[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA3 | 7:0  | DATA3 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA4 (0x39)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA4[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA4 | 7:0  | DATA4 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA5 (0x3A)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA5[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA5 | 7:0  | DATA5 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA6 (0x3B)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA6[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA6 | 7:0  | DATA6 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_DATA7 (0x3C)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_DATA7[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                  |
|--------------|------|------------------------------------------------------------------------------|
| TX_WPC_DATA7 | 7:0  | DATA7 of packet that is received by ASK demodulation in Tx (PeerPower) mode. |

**TX\_WPC\_CHECKSUM (0x3D)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | TX_WPC_CHECKSUM[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000          |   |   |   |   |   |   |   |
| Access Type | Read Only            |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                                                           |
|-----------------|------|-----------------------------------------------------------------------|
| TX_WPC_CHECKSUM | 7:0  | CHECKSUM of data received by ASK demodulation in Tx (PeerPower) mode. |

**FOD\_X0 (0x3E)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X0   | 7:0  | FOD Adjust Parameter |

**FOD\_Y0 (0x3F)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_0001 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y0   | 7:0  | FOD Adjust Parameter |

**FOD\_X1 (0x40)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_1000 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X1   | 7:0  | FOD Adjust Parameter |

**FOD\_Y1 (0x41)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_1010 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y1   | 7:0  | FOD Adjust Parameter |

**FOD\_X2 (0x42)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_1110 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X2   | 7:0  | FOD Adjust Parameter |

**FOD\_Y2 (0x43)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0010_0000 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y2   | 7:0  | FOD Adjust Parameter |

**FOD\_X3 (0x44)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X3[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_0000 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X3   | 7:0  | FOD Adjust Parameter |

**FOD\_Y3 (0x45)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y3[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_1111 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y3   | 7:0  | FOD Adjust Parameter |

**FOD\_X4 (0x46)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X4[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_0111 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X4   | 7:0  | FOD Adjust Parameter |

**FOD\_Y4 (0x47)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y4[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0010_0110 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y4   | 7:0  | FOD Adjust Parameter |

**FOD\_X5 (0x48)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X5[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_1101 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X5   | 7:0  | FOD Adjust Parameter |

**FOD\_Y5 (0x49)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y5[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0010_1100 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y5   | 7:0  | FOD Adjust Parameter |

**FOD\_X6 (0x4A)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X6[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0010_1010 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X6   | 7:0  | FOD Adjust Parameter |

**FOD\_Y6 (0x4B)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y6[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0011_1000 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y6   | 7:0  | FOD Adjust Parameter |



**FOD\_X7 (0x4C)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X7[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0011_0001 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X7   | 7:0  | FOD Adjust Parameter |

**FOD\_Y7 (0x4D)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y7[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0011_1110 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y7   | 7:0  | FOD Adjust Parameter |

**FOD\_X8 (0x4E)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X8[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0011_1100 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X8   | 7:0  | FOD Adjust Parameter |

**FOD\_Y8 (0x4F)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y8[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0100_0101 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y8   | 7:0  | FOD Adjust Parameter |

**FOD\_X9 (0x50)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_X9[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0100_1100 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X9   | 7:0  | FOD Adjust Parameter |

**FOD\_Y9 (0x51)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | FOD_Y9[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_0011 |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y9   | 7:0  | FOD Adjust Parameter |

**FOD\_X10 (0x52)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_X10[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_0011  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X10  | 7:0  | FOD Adjust Parameter |

**FOD\_Y10 (0x53)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_Y10[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_1000  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y10  | 7:0  | FOD Adjust Parameter |

**FOD\_X11 (0x54)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_X11[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_1001  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X11  | 7:0  | FOD Adjust Parameter |

**FOD\_Y11 (0x55)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_Y11[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_1110  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y11  | 7:0  | FOD Adjust Parameter |

**FOD\_X12 (0x56)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_X12[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0111_0111  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X12  | 7:0  | FOD Adjust Parameter |

**FOD\_Y12 (0x57)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_Y12[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0111_1100  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y12  | 7:0  | FOD Adjust Parameter |

**FOD\_X13 (0x58)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_X13[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1000_0110  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X13  | 7:0  | FOD Adjust Parameter |

**FOD\_Y13 (0x59)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_Y13[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1000_1011  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y13  | 7:0  | FOD Adjust Parameter |

**FOD\_X14 (0x5A)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_X14[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1001_0101  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X14  | 7:0  | FOD Adjust Parameter |

**FOD\_Y14 (0x5B)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_Y14[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1001_1011  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y14  | 7:0  | FOD Adjust Parameter |

**FOD\_X15 (0x5C)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_X15[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1010_0100  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_X15  | 7:0  | FOD Adjust Parameter |

**FOD\_Y15 (0x5D)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | FOD_Y15[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b1010_1011  |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION          |
|----------|------|----------------------|
| FOD_Y15  | 7:0  | FOD Adjust Parameter |

**OV\_CLAMP\_VOLTAGE (0x62)**

| BIT         | 7             | 6 | 5 | 4                 | 3             | 2 | 1                     | 0 |
|-------------|---------------|---|---|-------------------|---------------|---|-----------------------|---|
| Field       | RESERVED[2:0] |   |   | POV_CLAMP_VOLTAGE | RESERVED[1:0] |   | OV_CLAMP_VOLTAGE[1:0] |   |
| Reset       | 0b000         |   |   | 0b0               | 0b00          |   | 0b00                  |   |
| Access Type | Write, Read   |   |   | Write, Read       | Write, Read   |   | Write, Read           |   |

| BITFIELD          | BITS | DESCRIPTION                                              |
|-------------------|------|----------------------------------------------------------|
| RESERVED          | 7:5  | RSVD                                                     |
| POV_CLAMP_VOLTAGE | 4    | 1: OV_CLAMP_VOLTAGE - 1.5V<br>0: OV_CLAMP_VOLTAGE - 1.0V |
| RESERVED          | 3:2  | RSVD                                                     |
| OV_CLAMP_VOLTAGE  | 1:0  | 00: 17V<br>01: 16V<br>10: 15V<br>11: 14V                 |

**TX\_LAST\_CEP (0x63)**

| BIT         | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field       | TX_LAST_CEP[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000      |   |   |   |   |   |   |   |
| Access Type | Read Only        |   |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                           |
|-------------|------|-----------------------------------------------------------------------|
| TX_LAST_CEP | 7:0  | The latest received CEP from the WPC receiver in Tx (PeerPower) mode. |

**TX\_LAST\_RPP (0x64)**

| BIT         | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field       | TX_LAST_RPP[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000      |   |   |   |   |   |   |   |
| Access Type | Read Only        |   |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                           |
|-------------|------|-----------------------------------------------------------------------|
| TX_LAST_RPP | 7:0  | The latest received RPP from the WPC receiver in Tx (PeerPower) mode. |

**TX\_LAST\_PCHP (0x65)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | TX_LAST_PCHP[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0101       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                            |
|--------------|------|--------------------------------------------------------------------------------------------------------|
| TX_LAST_PCHP | 7:0  | The latest received PCHP (power control hold off packet) from the WPC receiver in Tx (PeerPower) mode. |

**LDO\_WPDET\_CNFG (0x70)**

| BIT         | 7                      | 6 | 5                      | 4 | 3                       | 2 | 1                       | 0 |
|-------------|------------------------|---|------------------------|---|-------------------------|---|-------------------------|---|
| Field       | WPDET_H_DE-BOUNCE[1:0] |   | WPDET_L_DE-BOUNCE[1:0] |   | WPDET_H_THRESH-OLD[1:0] |   | WPDET_L_THRESH-OLD[1:0] |   |
| Reset       | 0b01                   |   | 0b01                   |   | 0b01                    |   | 0b00                    |   |
| Access Type | Write, Read            |   | Write, Read            |   | Write, Read             |   | Write, Read             |   |

| BITFIELD           | BITS | DESCRIPTION                                  |
|--------------------|------|----------------------------------------------|
| WPDET_H_DE-BOUNCE  | 7:6  | 00: 1μs<br>01: 1ms<br>10: 2ms<br>11: 3ms     |
| WPDET_L_DEBOUNCE   | 5:4  | 00: 1μs<br>01: 1ms<br>10: 2ms<br>11: 3ms     |
| WPDET_H_THRESH-OLD | 3:2  | 00: 4.4V<br>01: 4.5V<br>10: 4.6V<br>11: 4.7V |
| WPDET_L_THRESH-OLD | 1:0  | 00: 3.6V<br>01: 3.8V<br>10: 4.0V<br>11: 4.2V |

**VRECT\_TARGET\_X0 (0xBA)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                                      |
|-----------------|------|--------------------------------------------------|
| VRECT_TARGET_X0 | 7:0  | V <sub>RECT</sub> Target Profile, X-coordinate 0 |

**VRECT\_TARGET\_Y0 (0xBB)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0111_0111          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                                          |
|-----------------|------|------------------------------------------------------|
| VRECT_TARGET_Y0 | 7:0  | V <sub>RECT</sub> Target Profile, WPC Y-coordinate 0 |

**VRECT\_TARGET\_PMA\_Y0 (0xBC)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0111_1011              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                              |
|---------------------|------|------------------------------------------|
| VRECT_TARGET_PMA_Y0 | 7:0  | VRECT Target Profile, PMA Y-coordinate 0 |

**VRECT\_TARGET\_X1 (0xBD)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0111          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                          |
|-----------------|------|--------------------------------------|
| VRECT_TARGET_X1 | 7:0  | VRECT Target Profile, X-coordinate 1 |

**VRECT\_TARGET\_Y1 (0xBE)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0111_0010          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                              |
|-----------------|------|------------------------------------------|
| VRECT_TARGET_Y1 | 7:0  | VRECT Target Profile, WPC Y-coordinate 1 |

**VRECT\_TARGET\_PMA\_Y1 (0xBF)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0111_0111              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                              |
|---------------------|------|------------------------------------------|
| VRECT_TARGET_PMA_Y1 | 7:0  | VRECT Target Profile, PMA Y-coordinate 1 |

**VRECT\_TARGET\_X2 (0xC0)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_0001          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                          |
|-----------------|------|--------------------------------------|
| VRECT_TARGET_X2 | 7:0  | VRECT Target Profile, X-coordinate 2 |

**VRECT\_TARGET\_Y2 (0xC1)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_1100          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                              |
|-----------------|------|------------------------------------------|
| VRECT_TARGET_Y2 | 7:0  | VRECT Target Profile, WPC Y-coordinate 2 |

**VRECT\_TARGET\_PMA\_Y2 (0xC2)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y2[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0111_0001              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                              |
|---------------------|------|------------------------------------------|
| VRECT_TARGET_PMA_Y2 | 7:0  | VRECT Target Profile, PMA Y-coordinate 2 |

**VRECT\_TARGET\_X3 (0xC3)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X3[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0001_1110          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                          |
|-----------------|------|--------------------------------------|
| VRECT_TARGET_X3 | 7:0  | VRECT Target Profile, X-coordinate 3 |

**VRECT\_TARGET\_Y3 (0xC4)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y3[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_0110          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                              |
|-----------------|------|------------------------------------------|
| VRECT_TARGET_Y3 | 7:0  | VRECT Target Profile, WPC Y-coordinate 3 |



**VRECT\_TARGET\_PMA\_Y3 (0xC5)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y3[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_1010              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                              |
|---------------------|------|------------------------------------------|
| VRECT_TARGET_PMA_Y3 | 7:0  | VRECT Target Profile, PMA Y-coordinate 3 |

**VRECT\_TARGET\_X4 (0xC6)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X4[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0010_1110          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                          |
|-----------------|------|--------------------------------------|
| VRECT_TARGET_X4 | 7:0  | VRECT Target Profile, X-coordinate 4 |

**VRECT\_TARGET\_Y4 (0xC7)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y4[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_0000          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                              |
|-----------------|------|------------------------------------------|
| VRECT_TARGET_Y4 | 7:0  | VRECT Target Profile, WPC Y-coordinate 4 |

**VRECT\_TARGET\_PMA\_Y4 (0xC8)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y4[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_0010              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                              |
|---------------------|------|------------------------------------------|
| VRECT_TARGET_PMA_Y4 | 7:0  | VRECT Target Profile, PMA Y-coordinate 4 |

**VRECT\_TARGET\_X5 (0xC9)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X5[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0011_1111          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                          |
|-----------------|------|--------------------------------------|
| VRECT_TARGET_X5 | 7:0  | VRECT Target Profile, X-coordinate 5 |

**VRECT\_TARGET\_Y5 (0xCA)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y5[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_1010          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                                          |
|-----------------|------|------------------------------------------------------|
| VRECT_TARGET_Y5 | 7:0  | V <sub>RECT</sub> Target Profile, WPC Y-coordinate 5 |

**VRECT\_TARGET\_PMA\_Y5 (0xCB)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y5[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_1011              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                                          |
|---------------------|------|------------------------------------------------------|
| VRECT_TARGET_PMA_Y5 | 7:0  | V <sub>RECT</sub> Target Profile, PMA Y-coordinate 5 |

**VRECT\_TARGET\_X6 (0xCC)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X6[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_0001          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                                      |
|-----------------|------|--------------------------------------------------|
| VRECT_TARGET_X6 | 7:0  | V <sub>RECT</sub> Target Profile, X-coordinate 6 |

**VRECT\_TARGET\_Y6 (0xCD)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y6[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_1000          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                                          |
|-----------------|------|------------------------------------------------------|
| VRECT_TARGET_Y6 | 7:0  | V <sub>RECT</sub> Target Profile, WPC Y-coordinate 6 |

**VRECT\_TARGET\_PMA\_Y6 (0xCE)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y6[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_1001              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                                          |
|---------------------|------|------------------------------------------------------|
| VRECT_TARGET_PMA_Y6 | 7:0  | V <sub>RECT</sub> Target Profile, PMA Y-coordinate 6 |

**VRECT\_TARGET\_X7 (0xCF)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_X7[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0110_0110          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                          |
|-----------------|------|--------------------------------------|
| VRECT_TARGET_X7 | 7:0  | VRECT Target Profile, X-coordinate 7 |

**VRECT\_TARGET\_Y7 (0xD0)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_Y7[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_0111          |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION                              |
|-----------------|------|------------------------------------------|
| VRECT_TARGET_Y7 | 7:0  | VRECT Target Profile, WPC Y-coordinate 7 |

**VRECT\_TARGET\_PMA\_Y7 (0xD1)**

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | VRECT_TARGET_PMA_Y7[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0101_0111              |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD            | BITS | DESCRIPTION                              |
|---------------------|------|------------------------------------------|
| VRECT_TARGET_PMA_Y7 | 7:0  | VRECT Target Profile, PMA Y-coordinate 7 |

**PMA\_ADV\_DATA (0xDB)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | PMA_ADV_DATA[7:0] |   |   |   |   |   |   |   |
| Reset       | 0b0000_0000       |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

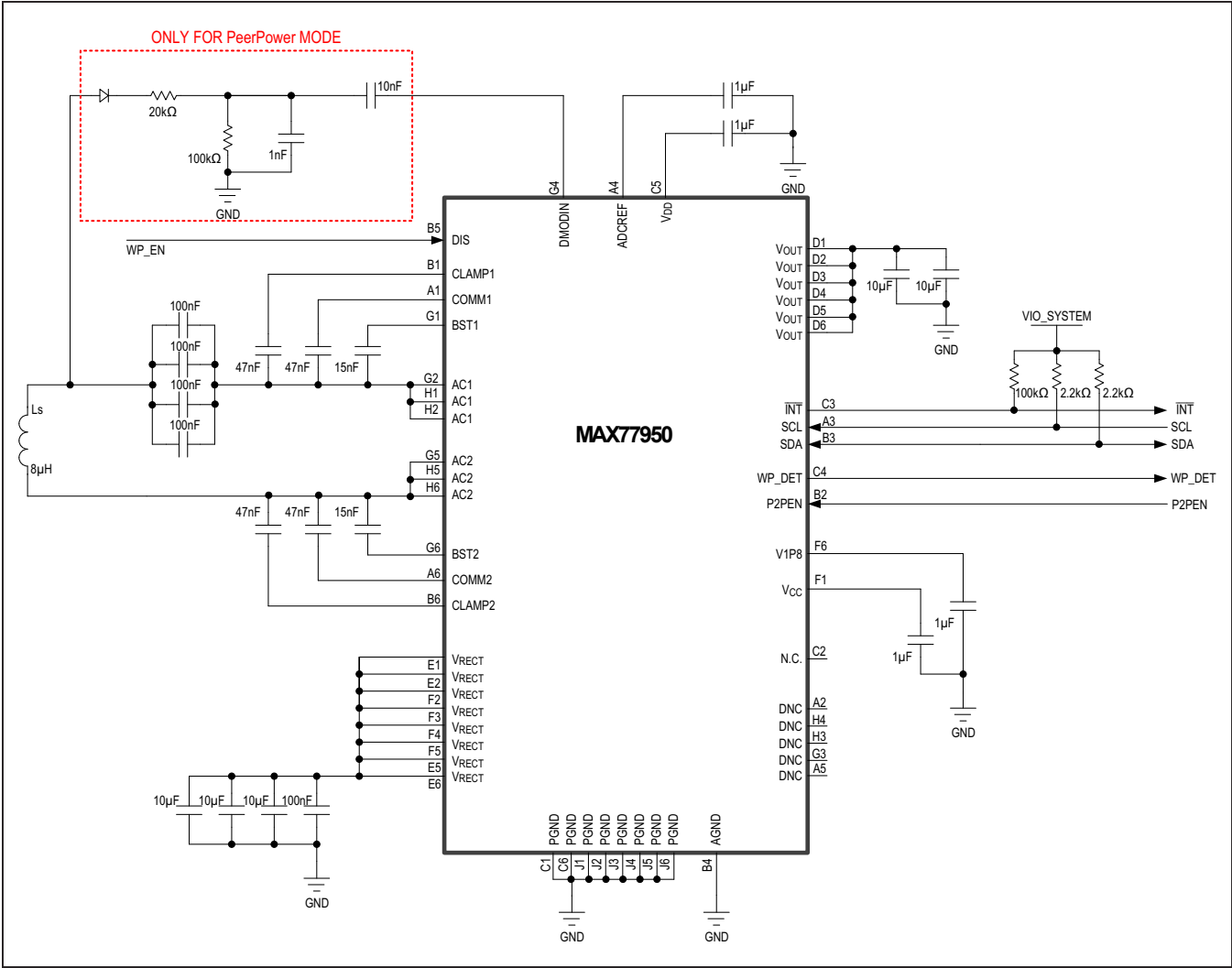
| BITFIELD     | BITS | DESCRIPTION                                                               |
|--------------|------|---------------------------------------------------------------------------|
| PMA_ADV_DATA | 7:0  | Data from the PMA advertisement packet received from the PMA transmitter. |

**PMA\_ADV\_CRC (0xDC)**

| BIT         | 7             | 6 | 5 | 4 | 3                | 2 | 1 | 0 |
|-------------|---------------|---|---|---|------------------|---|---|---|
| Field       | RESERVED[3:0] |   |   |   | PMA_ADV_CRC[3:0] |   |   |   |
| Reset       | 0b0000        |   |   |   | 0b0000           |   |   |   |
| Access Type | Read Only     |   |   |   | Read Only        |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                              |
|-------------|------|--------------------------------------------------------------------------|
| RESERVED    | 7:4  | RSVD                                                                     |
| PMA_ADV_CRC | 3:0  | CRC code in the PMA advertised packet received from the PMA transmitter. |

Typical Application Circuit



Ordering Information

| PART NUMBER   | TEMP RANGE     | PIN-PACKAGE                 |
|---------------|----------------|-----------------------------|
| MAX77950EWW+T | -40°C to +85°C | 52-bump WLP,<br>0.4mm pitch |

+ Denotes a lead(Pb)-free/RoHS-compliant package.  
T = Tape-and-reel.

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION     | PAGES<br>CHANGED |
|--------------------|------------------|-----------------|------------------|
| 0                  | 3/17             | Initial release | —                |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,  
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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